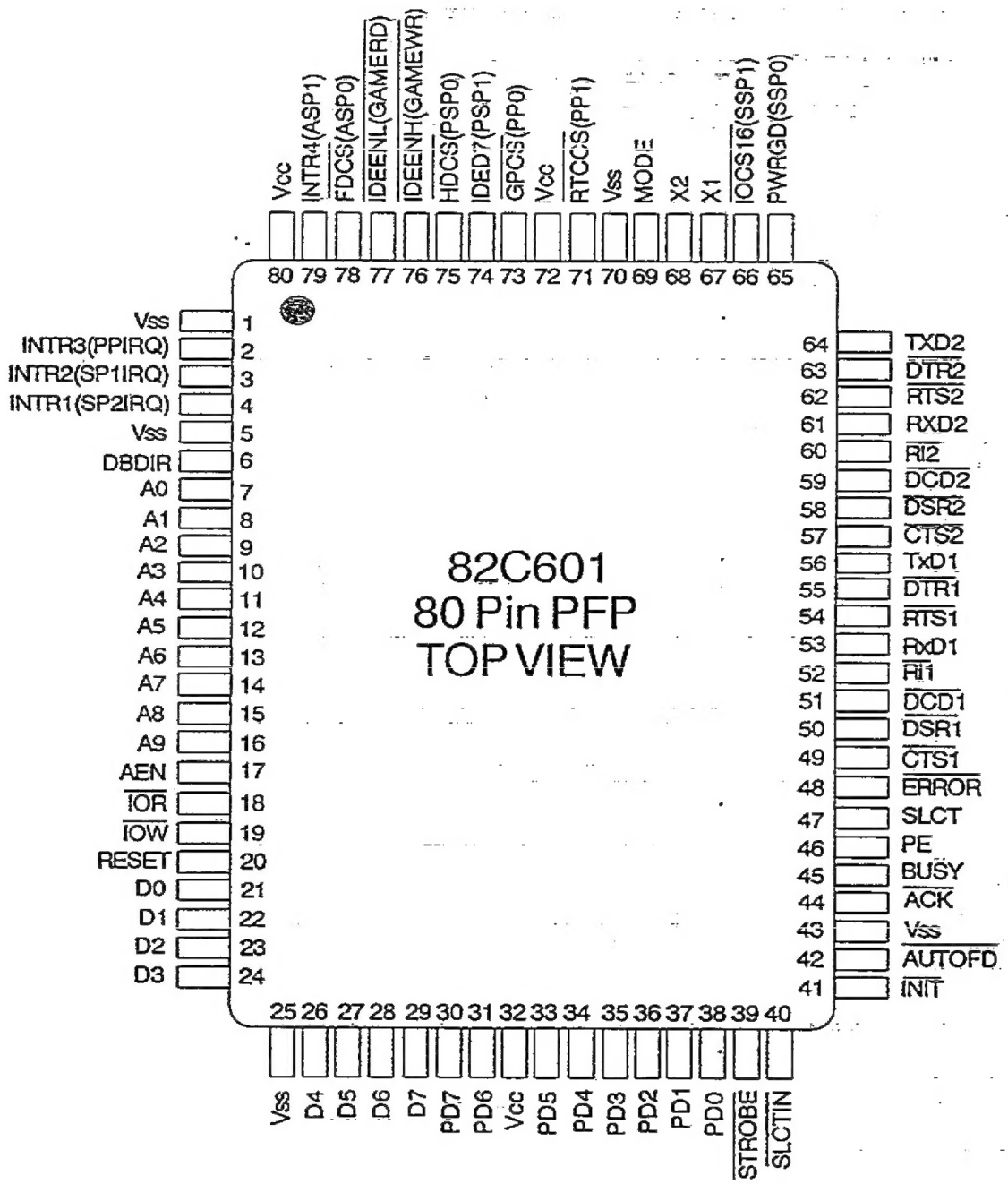
Chips and Technologies, Inc.

82C601
Single Chip Peripheral Controller

Advance Product Information

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production.

Rev. 6.0 8/30/90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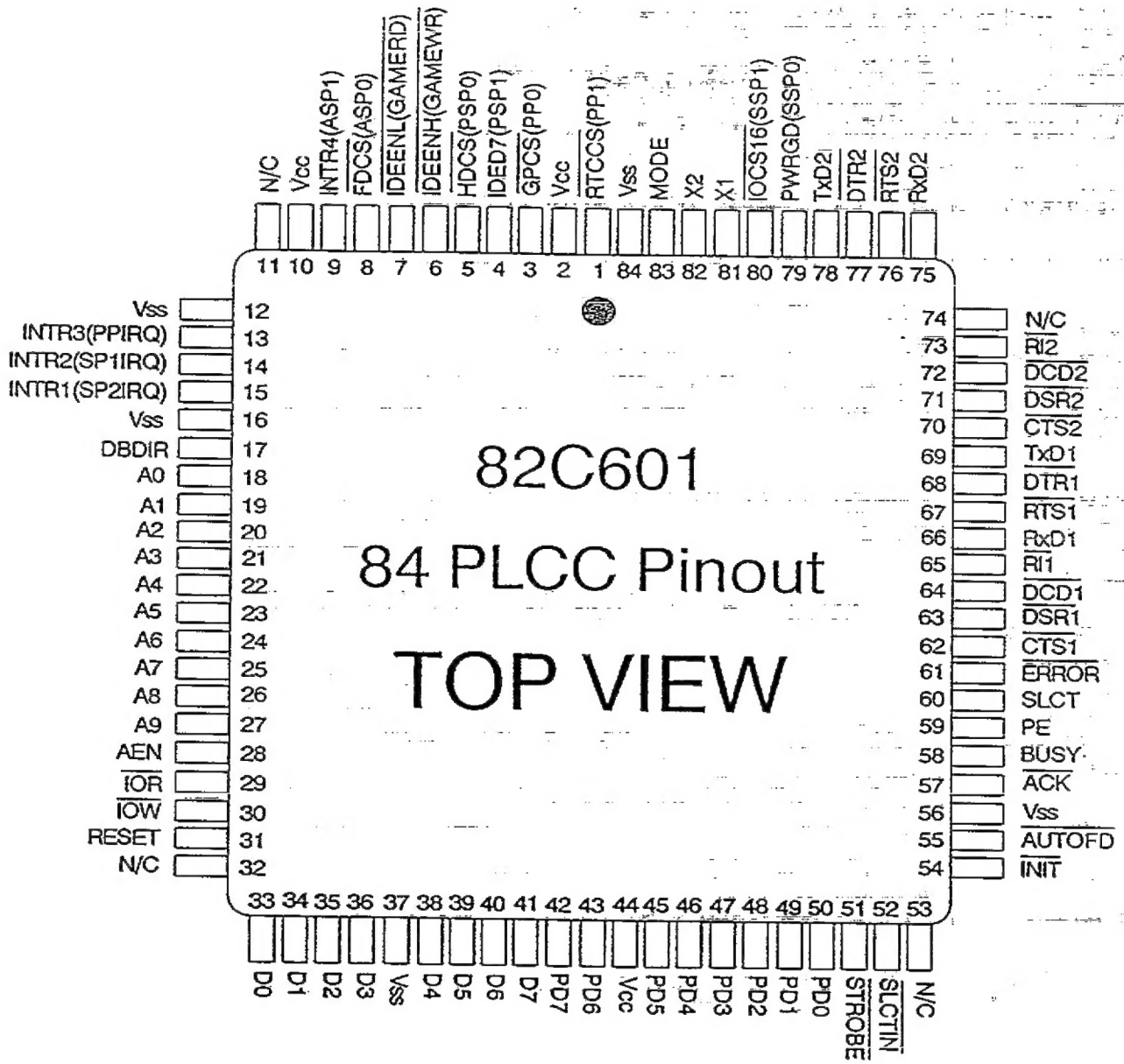
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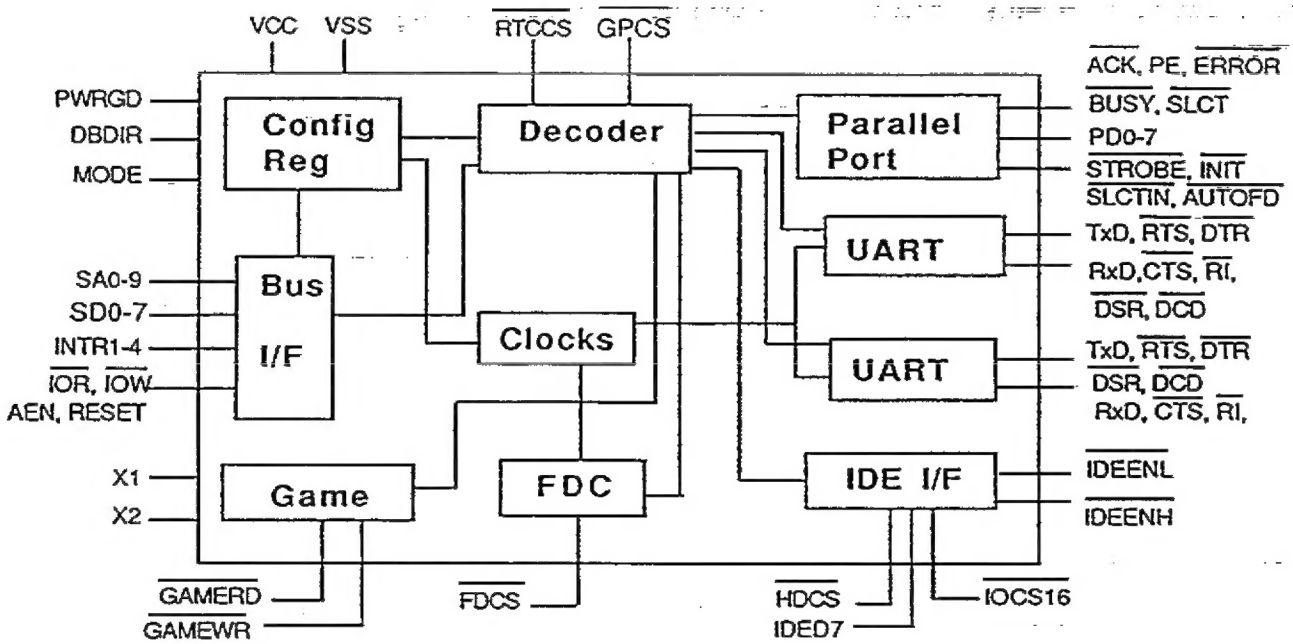
- 100% Compatible to IBM PC-Xt/AT
- 2 X 16450 Compatible UARTs
- 1 IBM PC-XT/AT Compatible Enhanced Parallel Port
- Dual Operating Modes
- MOTHERBOARD mode functions:
  - IDE Interface
  - Real Time Clock Chip Select
  - Programmable General Purpose Chip Select
  - Power Saving Features and Power Down Modes
- ADAPTER mode functions:
  - Game Port Decodes
  - Select Pins for Serial and Parallel Ports
- 16 mA Output Drivers
- Schmitt Trigger Inputs on RESET
- Internal Address Decoders
- EISA Ready (MOTHERBOARD mode)
  - Relocatable Ports
  - Relocatable IRQ
  - Interrupt Sharing Capability
- Low Power CMOSt
- 80 PFP or 84 PLCC Packages

82C601 BLOCK DIAGRAM



GENERAL DESCRIPTION

The 82C601 single chip peripheral controller is the second generation of our Multifunction Controller product line.

This chip is an LSI implementation of the most commonly used peripheral devices found in an IBM PC, XT or AT. The chip features 16 mA drivers for the output buffers, such as the host data bus and parallel port data bus. It incorporates two 16450 compatible UARTs, one enhanced parallel port (with bi-directional capability), and IDE compatible hard disk interface and various chip selects (in the MOTHERBOARD Application) or select pins and Game port decodes (in the ADAPTER Application). Decoding logic and support for main, auxiliary and standby power supplies and software configurable base addres ss for these devices, operational modes and interrupts are also included. This chip supports 2 applications:

- MOTHERBOARD Application where all the ports are relocatable. An Integrated Drive Electronics interface, and various Chip Selects (Floppy Disk, Real Time Clock, and a General Purpose) have been added for this mode. Power management aspects of the 82C601 in the MOTHERBOARD Application includes modular power down for each port, oscillator disable, and chip power down through the PWRGD pin. When the chip is powered down (i.e. when PWRGD is inactive) the current draw should be less than 50 micro-Amps, all the inputs are disabled, and all outputs are tri-stated. The contents of all the registers are preserved, as long as power supply to the 82C601 is maintained.

- ADAPTER Application where the base addresses for the ports are determined by the select pins (PSPs, SSPs, ASPs, and PPS); except for game port, it is fixed @ 200H-207H. -GAMERD and -GAMEWR outputs are provided to minimize external gate count.

The host interface is PC compatible, i.e. D0-D7, A0-A9, -IOR, -IOW, AEN, INTR1, INTR2, INTR3, INTR4, and RESET, and can be connected directly to the bus. The data buffers (D0-D7, PD0-PD7, IDED7) are capable of sinking 16 mA @ 0.5 V, the parallel port control signals are open collector with internal pull up resistors; and are capable of sinking 16 mA @ 0.5 V.

The UARTs implement fully functional serial links. Programmable character length, parity generation and detection, stop-bit generation and baud rate generation are provided. Double buffering is used so that precise synchronization is unnecessary. Status information is accessible to the CPU by reading internal registers. MODEM control lines are provided, as are internal diagnostic functionality and interrupt prioritization. Support for an auxiliary power system (such as that derived from a telephone line or RS232 link) permits an 82C601 in a battery-powered device to consume no battery power until an incoming character is detected.

The parallel port can be configured for output only (printer application) or input and output(bi-direction).

The configuration RAM and circuitry support programmable base addresses for all registers internal to the chip. This permits creation of a menu-driven program for system configuration. Selection of sources for interrupts, enabling and configuring of on-chip subsystems (UARTs, parallel port, etc.) and control of the configuration process itself are also handled with this RAM and its associated circuitry.

The remainder of this data sheet will consider each of the aforesaid subsystems individually. Sections containing more general design data for the chip as a whole are at the end along with electrical and physical characteristics.

Figure 1 depicts the subsystems present in the 82C601.

1.0 82C601 PIN DESCRIPTIONS

PIN NUMBER PLCC(PFP)	PIN SYMBOL	BUFFER TYPE	DESCRIPTION
1.1 HOST INTERFACE (27 pins)			
9 (79)	INTR4 (Interrupt Request)	T	Active high Interrupt Request. MOTHERBOARD function. When the parallel port is assigned to be LPT1 (I/O address 3BCH) or LPT3 (I/O address 378H), INTR4 generates interrupt to the host, normally connected to IRQ7. If I/O address 278H is selected, then the parallel port is assigned to be LPT2, therefore it should use IRQ5. INTR4 originates from either the Secondary Serial Port or the Parallel Port Controller.
	(ASP1) (Alternate Serial Port Select)	I	Alternate Serial Port Select 1, ADAPTER Application function. ASP0 (pin 8(78)) and ASP1 determines the Serial Port addresses for COM3 and COM4.
13 (2)	INTR3 (Interrupt Request)	T	Active high Interrupt Request, MOTHERBOARD function. In the MOTHERBOARD Application, INTR3 originates from the Primary Serial Port or the Parallel Port Controller.
	(PPIRQ) Parallel Port Interrupt	T	Active high Parallel Port Interrupt, ADAPTER Application. In the ADAPTER Application, this pin should be connected to the IRQ5 when the parallel port is assigned to be LPT2 (I/O address 278H).
14 (3)	INTR2 (Interrupt Request)	T	Active high Interrupt Request, MOTHERBOARD function. In the MOTHERBOARD Application, INTR2 originates from the Primary Serial Port or the Secondary Serial Controller.
	(SP1IRQ) (Primary Serial Port Interrupt)	T	Active high Primary Serial Port Interrupt, ADAPTER function. In the ADAPTER Application, SP1IRQ is normally connected to IRQ4 for COM1/COM3.
15 (4)	INTR1 (Interrupt Request)	T	Active high Interrupt Request, MOTHERBOARD function. In the MOTHERBOARD Application, INTR1 originates from the Primary Serial Port or the Secondary Serial Port.
	(SP2IRQ) (Secondary Serial Port Interrupt)	T	Active high Secondary Serial Port Interrupt, ADAPTER function. In the ADAPTER Application, SP2IRQ is normally connected to IRQ3 for COM2/COM4.
17 (6)	DBDIR (Data Bus Direction)	O	Host Data Bus Buffer Direction. Active high signal indicates read cycle for 82C601 internal accesses, Parallel port, Serial port and FDC. Also goes high if IDE, Real Time Clock Chip Select (-RTCCS) and General Purpose Chip Select (-GPCS) are active and their buffer modes are enabled (through configuration register).
18..27 (7..16)	A0-A9 (I/O Address)	I	Host address bit 0-9. These address bits are latched internally at the beginning of -IOR or -IOW.
28 (17)	AEN (Address Enable)	I	Active high Address Enable indicates DMA activity. Normally, this signal is used with A0-A9,-IOW,-IOR to decode I/O address ports.
29 (18)	-IOR (I/O Read)	I	Active low I/O read from host.
30 (19)	-IOW (I/O Write)	I	Active low I/O write from host.
31 (20)	RESET (Master Reset)	IS	Active high Reset from host (Schmitt-trigger input). RESET has to be valid for a minimum of 500 nanosecond. This resets the serial port, parallel port, and the FDC. The effect of hardware reset is shown in the functional description of each port. The configuration registers are not affected. They come up in the default condition only on power up.
33-36, 38-41 (21-24, 26-29)	D0-D7 (Data Bus)	I/OH	Host data bus, 16 mA driver. This bi-directional data bus is used to transfer information between the CPU and 82C601.

PIN NUMBER	PIN SYMBOL	BUFFER TYPE	DESCRIPTION
1.2 PARALLEL PORT CONTROLLER (17 pins):			
42,43,45-50 (30,31, 33-38)	PD7-PD0 (Port Data)	I/OH	The bi-directional parallel data bus is used to transfer information between CPU and peripherals. These signals have high current drive and capable of sinking 16mA @ 0.5V
51 (39)	-STROBE (Data Strobe)	OC	This active low output indicates to the peripheral that the data at the parallel port is valid. This pin has high current drive and is capable of sinking 16 mA @ 0.5V.
52 (40)	-SLCTIN (Select Input)	OC	This active low output selects the printer when it is low. This pin has high current drive and is capable of sinking 16 mA @ 0.5V.
54 (41)	-INIT (Initialize)	OC	This active low output initializes (reset) the printer when it is low. This pin has high current drive and is capable of sinking 16mA @ 0.5V.
55 (42)	-AUTOFD (Automatic Feed)	OC	When this output is low the printer automatically adds one line feed after printing. This pin has high current drive and is capable of sinking 16 mA @ 0.5V.
57 (44)	-ACK (Acknowledge)	I	Active low Acknowledge input. Low indicates that data has been received and the printer is ready to accept more data.
58 (45)	BUSY (Printer Busy)	I	Active high Busy input. The high input signal indicates the printer can not accept additional data.
59 (46)	PE (Paper End)	I	Active high Paper End input. The high input signal indicates the printer is out of paper.
60 (47)	SLCT (Select)	I	Active high device Select input. The input is set high by the printer when it is selected.
61 (48)	-ERROR (Error)	I	Active low Error input. This input is set low by the printer when it detects the error.
1.3 SERIAL PORT INTERFACE (18 pins)			
62, 70 (49, 57)	-CTS1, -CTS2 (Clear to Send)	I	Active low Clear to Send input. Handshake signal which notifies the UART that the MODEM is ready to receive data. The CPU can monitor the status of -CTS signal by reading bit 4 of Modem Status Register (MSR). A -CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when -CTS changes state. The -CTS signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of -CTS.
63, 71 (50, 58)	-DSR1, -DSR2 (Data Set Ready)	I	Active low Data Set Ready input. Handshake signal which notifies the UART that the MODEM is ready to establish the communication link. The CPU can monitor the status of -DSR signal by reading bit 5 of Modem Status Register. A -DSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when -DSR changes state. Note: Bit 5 of MSR is the complement of -DSR.
64, 72 (51, 59)	-DCD1, -DCD2 (Data Carrier Detect)	I	Active low Data Carrier Detect input. Handshake signal which notifies the UART that carrier signal is detected by the MODEM. The CPU can monitor the status of -DCD signal by reading bit 7 of Modem Status Register (MSR). A -DCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when -DCD changes state. Note: Bit 7 of MSR is the complement of -DCD.

PIN NUMBER	PIN SYMBOL	BUFFER TYPE	DESCRIPTION
65, 73 (52, 60)	-RI1, -RI2 (Ring Indicator)	I	Active low Ring Indicator input. Handshake signal which notifies the UART that a telephone ring signal is detected by the MODEM. The CPU can monitor the status of -RI signal by reading bit 6 of Modem Status Register (MSR). A -RI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when -RI changes state. Note: Bit 6 of MSR is the complement of -RI.
66, 75 (53, 61)	RXD1, RXD2 (Receive Data)	I	Active high receive serial data input from communication link.
67, 76 (54, 62)	-RTS1, -RTS2 (Request to Send)	O	Active low Request To Send output. Handshake output signal notifies MODEM that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the -RTS signal to inactive mode (high). Forced inactive during loop mode operation.
68, 77 (55, 63)	-DTR1, -DTR2 (Data Terminal Ready)	O	Active low Data Terminal ready output. Handshake output signal notifies MODEM that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the -DTR signal to inactive mode (high). Forced inactive during loop mode operation.
69, 78 (56, 64)	TXD1, TXD2 (Transmit Data)	O	Active high transmit serial data output to the communication link.
81, (67)	X1(Crystal Clock)	I	Serial Port crystal input, normally 1.8432 MHz.
82 (68)	X2(Crystal)	OL	Serial Port crystal output.

1.4 IDE INTERFACE AND CHIP SELECTS (MOTHERBOARD Application) (10 PINS) CONFIGURATION SELECTS (ADAPTER Application)

79 (65)	PWRGD (Power good)	I	Active high Power Good indication, MOTHERBOARD AT/XT mode. The 82C601 is fully functional when PWRGD is active; when PWRGD is inactive and Vcc is still valid, the 82C601 is isolated from the rest of the circuit. All accesses are ignored, all inputs are disabled, and all outputs are tri-stated. However, register contents are preserved, and the current draw is minimal.
	(SSP0) (Secondary Serial Port Select 0)	I	Secondary Serial Port Select 0, ADAPTER Application.
80 (66)	-IOCS16 (16 bit I/O Indication)	I	Active low 16 bit I/O indication, MOTHERBOARD AT mode. The hard disk interface generates -IOCS16 to inform the host and the 82C601 that 16 bit I/O transfers are about to begin. -IOCS16 is active only when transferring data words in AT mode. Low = 16 bit, high = 8 bit (AT mode).
	(-HDACK)	I	Active Low HDC DMA Acknowledge, MOTHERBOARD XT mode.
	(SSP1) (Secondary Serial Port Select 1)	I	Secondary Serial Port Select 1, ADAPTER MODE. SSP0 and SSP1 select the address assignment for the second serial port.

SSP1	SSP0	IRQ	Address
0	0	IRQ3	2F8H (COM2)
0	1	IRQ4	COM3, the address is assigned by AS1, AS0
1	0	IRQ3	COM4, the address is assigned by AS1, AS0
1	1	–	Disabled

PIN NUMBER	PIN SYMBOL	BUFFER TYPE	DESCRIPTION
4 (74)	IDED7 (IDE Data Bit 7)	I/OH	IDE Data Bit 7, MOTHERBOARD AT mode, 16 mA driver. IDED7 transfers data @ I/O addresses 1F0H-1F7H (R/W), 3F6H (R/W), 3F7 (W). IDED7 should be connected to the IDE data bit 7. Normally, the 82C601 functions as a buffer, transferring data bit 7 between the IDE device and the host. Except during read of I/O address 3F7H, D7 is tri-stated, and data bits 0-6 are sourced by the hard disk interface.
	(RSVD)	N/A	Not used in MOTHERBOARD XT mode
	(PSP1) (Primary Serial Port Select 1)	I	Primary Serial Port Select 1, ADAPTER MODE. PSP0 and PSP1 select the address assignment for the primary serial port.

PSP1	PSP0	IRQ	Address
0	0	IRQ4	3F8H (COM1)
0	1	IRQ3	2F8H (COM2)
1	0	IRQ4	COM3, the address is assigned by AS1, AS0
1	1	–	Disabled

5 (75)	-HDCS (Hard Disk Chip Select)	OH	Active low Hard Disk Chip Select, MOTHERBOARD AT/XT mode. -HDCS decodes the primary HDC; default is I/O address 1F0H-1F7H (AT mode, CR#0CH <6> =0) or 320H-323H (XT mode, CR#0CH<6> = 1).
	(PSP0) (Primary Serial Port Select 0)	I	Primary Serial Port Select 0, ADAPTER MODE. PSP0 and PSP1 select the address assignment for the primary serial port.
6 (76)	-IDEENH (High Data Buffer Enable)	OH	Active low High Data Buffer Enable, MOTHERBOARD AT mode. -IDEENH is active only when -IOCS16 is active, I/P address 1F0H-1F7H, and AT mode is selected.
	(RSVD)	N/A	Not Used in MOTHERBOARD XT mode.
	(-GAMEWR) (Game Write)	O	Active low Game Write strobe, ADAPTER Application. -GAMEWR decodes I/O address range 200H-207H and qualifies it with -IOW.
7 (77)	-IDEENL (Low Data buffer Enable)	O	Active low Low Data buffer Enable, MOTHERBOARD AT/XT mode. -IDEENL is active when accessing I/O address 1F0H-1F7H and 3F6H-3F7H (AT mode) or 320H-323H (XT mode: 8 bit DMA or programmed I/O).
	(-GAMERD) (GAME READ)	O	Active low Game Read strobe, ADAPTER Application. -GAMERD decodes I/O address range 200H-207H and qualifies it with -IOR.
1 (71)	-RTCCS (Real Time Clock Chip Select)	O	Active low Real Time Clock Chip Select, MOTHERBOARD AT/XT mode. -RTCCS decodes I/O addresses 70H and 71H for the 146818 compatible RTC.
	(PP1) (Parallel Port Select 1)	I	Parallel Port Select 1, ADAPTER Application. PP0 and PP1 determine the base address for the parallel port controller.

PP1	PP0	IRQ	Address
0	0	IRQ5	3BCH (LPTA)
0	1	IRQ5	278H (LPTC)
1	0	IRQ7	378H (LPTB)
1	1	–	Disabled

3 (73)	-GPCS (General Purpose Chip Select)	O	Active low General Purpose Chip Select, MOTHERBOARD AT/XT mode. -GPCS decodes the address specified in the Config. Reg. #09H and #0AH with the mask bit specified in the Config. Reg. 0AH.
	(OUT1)	O	OUT1 output from the Primary Serial Port, when CR#0Bh<0>=1.
	(PP0) (Parallel Port Select 0)	I	Parallel Port Select 0, ADAPTER Application. PP0 and PP1 determine the base address for the parallel port controller.
8 (78)	-FDCS (Floppy Disk Chip Select)	OH	Active low Floppy Disk Chip Select, MOTHERBOARD AT/XT mode. -FDCS decodes the primary Floppy Disk @ address 3F0H-3F7H.
9 (79)	ASP0 (Alternate Serial Port Select)	I	Alternate Serial Port Select 0, ADAPTER Application.
	(ASP1) (Alternate Serial Port Select)	I	Alternate Serial Port Select 1, ADAPTER Application. ASP0 and ASP1 select the base address pairs for the primary and secondary serial port when they are used as COM3, COM4 pair.

ASP1	ASP0	COM3	COM4
0	0	338H	238H
0	1	3E8H	2E8H
1	0	2E8H	2E0H
1	1	220H	228H

1.5 Miscellaneous

83 (69)	MODE (Mode Select)	I	Mode Select. 0 = MOTHERBOARD Application. MOTHERBOARD Application allows you to configure the 82C601 and fully utilize the power management functions. 1 = ADAPTER Application. In the ADAPTER Application the port addresses are determined by the jumper selects, except for the game port, which is fixed at address 200H-207H.

1.6 POWER AND GROUND (8 PINS)

2, 10, 44 (32, 72, 80)	Vcc (3) (Power)	+5V Digital supply pins
12,16,37,56,84 (1,5,25,43,70)	Vss (5) (Ground)	0V Reference for the CPU interface, serial port, parallel port, and disk interface output drive circuitry, respectively.
11,32,53,74	No Connect	

Buffer Types:	I	=	TTL input
	IS	=	Schmitt-trigger input
	O	=	TTL output
	OH	=	High current TTL output
	OC	=	Open Drain
	OL	=	Low current open drain output
	T	=	Tri-state TTL output, 24 mA

2.0 SERIAL PORT (UART)

2.1 Introduction

Two equivalent NS16450 UARTs are implemented on the 82C601. The serial ports are fully compatible to the 16450 ACE registers. The programmable features allow data rates ranging from 50 baud to 115.2 Kbaud; 5 to 8 bit character size with 1 start and 1, 1.5, 2 stop bits; even, odd, sticky, or no parity; and prioritized interrupts. An interrupt for each UART is enabled or disabled (tri-stated) using the OUT2 bit. If a 1 is written to OUT2, UART, interrupt is enabled. Writing 0 tri-states the interrupt. There is a difference between the Primary Serial Port and the Secondary Serial Port. OUT1 of Primary Serial Port can be selected to become an output. -GPCS output can be configured to be either OUT1 of the Primary Serial Port or a General Purpose Chip Select depending upon CR#0BH<0>. If CR#0BH=0, then pin 3 (73) is -GPCS (default); if CR#0BH=1, pin 3 (73) becomes the OUT1 pin of the Primary Serial Port.

Table 2.0 Addressing of UART Registers

DRAB	A2	A1	A0	OFFSET	REGISTER NAME
0	0	0	0	0H	Received Buffer Register (R)
0	0	0	0	0H	Transmit Buffer Register (W)
0	0	0	1	1H	Interrupt Enable Register (R/W)
X	0	1	0	2H	Interrupt Flag Register (R/W)
X	0	1	1	3H	Byte Format Register (R/W)
X	1	0	0	4H	Modem Control Register (R/W)
X	1	0	1	5H	Line Status Register (R/W)
X	1	1	0	6H	Modem Status Register (R/W)
X	1	1	1	7H	Scratch Pad Register (R/W)
1	0	0	0	0H	Divisor LSB (R/W)
1	0	0	1	1H	Divisor MSB (R/W)

Where:

X = Don't Care
MSB = Most Significant Byte
LSB = Least Significant Byte
DRAB = Divisor Register Address Bit (Bit 7 of Byte Format Register)

MOTHERBOARD Application

The serial port base address is relocated by writing different values to Configuration Register #04H and/or #05H. Interrupts for Primary Serial Port and Secondary Serial Port depend on the values written to the Interrupt Source Register (Configuration Register #08H). In this mode the serial port base addresses (CR#04H, CR#05H) and interrupt sources (CR#08H) are programmable.

ADAPTER Application:

The base addresses are determined by PSP0-1, SSP0-1, and ASP0-1 input combinations. ASP0 and ASP1 are used only when Primary Serial Port/Secondary Serial Port are selected to be COM3/COM4 pairs; these pins determine the address pairs. SP1IRQ is the interrupt for the Primary Serial Port, SP2IRQ is for the Secondary Serial Port, and PPIRQ is for the parallel port. Any of these interrupts can be jumpered to the appropriate IRQ lines. Customarily, the Primary Serial Port is assigned as COM1:3F8H-3FFH with SP1IRQ connected to IRQ4; and the Secondary Serial Port is assigned as COM2: 2F8H-2FFH, SP2IRQ is connected to IRQ3. SP1IRQ can be assigned to IRQ3, IRQ4, or IRQ5 pins; conversely SP2IRQ can be assigned to IRQ3, IRQ4, or IRQ7. But the Primary Serial Port interrupt can not be the same as the Secondary Serial Port designation, that is, interrupts cannot be shared in the ADAPTER Application.

PSP1	PSP0	Addr	SSP1	SSP0	Addr
0	0	3F8H	0	0	2F8H
0	1	2F8H	0	1	COM3
1	0	COM3	1	0	COM4
1	1	OFF	1	1	OFF

ASP1	ASP0	COM3	COM4
0	0	338H	238H
0	1	3E8H	2E8H
1	0	2E8H	2E0H
1	1	220H	228H

Note: COM3 and COM4 addresses are determined by ASP1, ASP0 combination.

An on-chip baud rate generator divides the input clock or crystal frequency by a number from 1 to 65535. This frequency is used for both receiving and transmitting serial data.

Serial-to-parallel conversion is performed on received data and parallel-to-serial conversion is performed on transmitted data. Status of the UART is available at any time. To access it, the CPU reads the appropriate status register in the chip. The current state and type of a transfer are contained in this status information as are details regarding any errors encountered. The conditions under which the processor will be interrupted and the interrupt line to be used are programmable.

Control lines are provided to permit interfacing to a MODEM. Internal diagnostics are supported that permit simulation of break, parity, overrun and framing error conditions as well as operation in loopback mode.

2.2 Serial Port Registers

Addressing of the accessible UART registers is shown in the Table 2.0. The base address of all registers is software programmable during the configuration sequence (see the section entitled "82C601 Configuration"). UART registers are located at sequentially increasing addresses above this base address. The 82C601 contains two UARTs which contain a set of the registers described below.

BIT DEFINITIONS OF SERIAL PORT REGISTERS

2.2.1 Receive Buffer (RB)
Offset=0H, Read only, DRAB=0

This register holds the incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Double buffering is supported by the 82C601. This scheme uses an additional shift register (the Receive Shift Register; not user accessible) to assemble the incoming byte before it is loaded into the Receive Buffer.

2.2.2 Transmit Buffer (TB)
Offset=0H, Write only, DRAB=0

This register holds the data byte to be sent. Bit 0 is the least significant bit, which is transmitted and received first. Double buffering is supported by the 82C601. This scheme uses a shift register (the Transmit Shift Register; not user accessible) which is loaded from the Transmit Buffer. The transmitted byte is then shifted out of the Transmit Shift Register to the TXD pin.

2.2.3 Divisor Low Byte
Offset=0H, Read/Write, DRAB=1

2.2.4 Interrupt Enable Register (IER)
Offset=1H, Read/Write, DRAB=0

The low order 4 bits of this register control the enabling of each of the four possible types of interrupts. Setting a bit to a logic 1 enables the corresponding interrupt. It is possible to enable all, none, or some of the interrupt sources. Disabling all interrupts means that the interrupt flag register content is not valid and that none of the interrupt signals output by the 82C601 can be triggered by a UART. All other portions of the UART are unaffected by the disabling of interrupts. The individual bit definitions are as follows:

Bit 0: A logic 1 here causes an interrupt when the Receive Buffer contains valid data.

Bit 1: A logic 1 here causes an interrupt when the Transmit Buffer is empty.

Bit 2: A logic 1 here causes an interrupt when an error (Overrun, Parity, Framing or Break) has been encountered. The Line Status register must be read to determine the type or error.

Bit 3: A logic 1 here causes an interrupt when one of the bits in the MODEM Status register changes state.

Bits 4-7: These four bits are not used and are set to 0.

2.2.5 Divisor High Byte
Offset=0H, Read/Write, DRAB=1

2.2.6 Interrupt Flag Register (IFR)
Offset=2H, Read Only, DRAB=X

When accessed, this register reports the highest pending interrupt. By reading it, the CPU can determine the source of the interrupt and can act accordingly. The Interrupt Flag Register (IFR) records the highest pending interrupt in bits 0 through 2. Other interrupts are temporarily disregarded (they are internally saved by the 82C601) until the highest priority one is serviced.

Four levels of prioritized interrupts exist. In descending order of priority they are:

1. Line Status (highest priority)
2. Receive Buffer full
3. Transmit Buffer empty
4. MODEM Status (lowest priority)

Bit definitions for the IFR are as follows:

Bit 0: If this bit is a zero, an interrupt is pending and bits 1 and 2 can be read to determine the source of the interrupt. When this bit is a logic 1, no interrupts are pending. Note that this bit can be used in a polled environment to determine if an interrupt is pending. It can also be used for the same purpose with a hardwired interrupt priority scheme. In the latter case, bits 1 and 2 of this register act as a pointer to an interrupt service routine.

Bits 1 and 2: As indicated in Table 2.1, these two bits specify the type and source of the interrupt.

Bits 3-7: These five bits are set to 0.

2.2.7 Byte Format Register (BFR)
Offset=3H, Read/Write, DRAB=X

This read/write register contains format information for the serial line. Since it can be read, a separate copy of its content need not be kept in system memory. Bit definitions are as follows:

Bits 0 and 1: These specify the word length for received and transmitted characters. Start, stop and parity bits are not included in the word length value. The word lengths are:

Bit 0	Bit 1	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: The combination of this bit and Bits 0 and 1 of this register determine the number of stop bits used with each transmitted character. The table below summarizes this information. Note that the receiver will ignore additional stop bits beyond the first regardless of the number of stop bits used when transmitting.

Bit 2	Word Length	Number of Stop Bits
0	——	1
1	5 Bits	1 1/2
1	6 Bits	2
1	7 Bits	2
1	8 Bits	2

Bit 3: Parity Enable
0 = Disable Parity, parity bit is not generated nor checked
1 = Enable Parity Logic

A logic 1 in this bit enables parity generation (during transmission) and checking (during receipt). The parity bit is always after the last data bit but before the first stop bit. If enabled, a parity bit of the proper state (0 or 1) is generated such that the sum (carry ignored) of all data bits plus the parity bit produces either an even (even parity) or odd (odd parity) value.

Bit 4: Parity Select, this bit is meaningless unless parity is enabled (b3 = 1)
0 = Odd Parity, default
1 = Even parity. Parity bit is 1 when there are even number of 1s

This Even Parity bit controls parity sense. It is ignored unless Bit 3 is a logic 1. If Bits 3 and 4 are logic 1s (even parity), an even number of logic 1s will be transmitted and a parity error will be generated each time an odd number is received. If Bit 3 is a 1 and Bit 4 is a 0 (odd parity), an odd number of logic 1s will be transmitted and a parity error will be generated each time an even number is received.

Bit 5: Sticky Parity Enable
0 = Disable Sticky Parity, default
1 = Enable Sticky Parity

This is the Force Parity bit. It ensures that the parity bit and sense (even or odd) match regardless of the sum normally used to determine parity. Thus if BFR Bits 3, 4 and 5 are all logic 1s (even parity), the parity bit transmitted will always be a 0 and a parity error will be detected if a logic 1 parity bit is received. If Bits 3 and 5 are 1 and Bit 4 is 0, the parity bit transmitted will always be a 1 and a parity error will be detected if a 0 parity bit is received.

b3	b4	b5	Description
0	x	x	No parity generated nor checked
1	0	0	Odd Parity
1	0	1	Parity bit is generated and checked as 1
1	1	0	Even Parity
1	1	1	Parity bit is generated and checked as 0

Bit 6: Break Control Enable
0 = Disable Break Control, default
1 = Enable Break Control, TxD is forced to 0

This BREAK bit, when set to a logic 1, forces the transmitted data output pin TXD to a Spacing or logic 0 condition. This BREAK condition is terminated when Bit 6 is set to a 0. The operation of the transmitter logic is unaffected by the value of this bit; only the value of the TXD pin is affected. A BREAK condition is typically used to alert a terminal in a communications system. To prevent the transmission of erroneous data, follow the steps below:

1. Load a NULL character (all zeroes) into the Transmit Buffer.
2. Load Bit 6 (BREAK bit) after the next Transmit Buffer Empty (TBE) occurs.
3. Time the length of the BREAK condition by continuing to load NULL characters into the Transmit Buffer and counting the number loaded.
4. Clear the BREAK condition only after a Transmitter Empty (TEMT) condition occurs.

Bit 7: Line Control Register
Divisor Register Enable Bit
0 = Disable Divisor Register and Enable Rx/Tx Register, default
1 = Enable Divisor Register and Disable Rx/Tx Register

This Divisor Register Address Bit (DRAB) must be a logic 1 to permit access to the Divisor Registers. Access to all other internal UART registers requires that this bit be 0.

2.2.8. Modem Control Register (MCR)
Offset=4H, Read/Write, DRAB=X

This byte-wide register is used to manage the connection to an external MODEM or data set. Bit definitions are as follows:

Bit 0: This -DTR bit determines the state of the -DTR output pin. Setting Bit 0 to a logic 1 forces -DTR to its active state (logic 0). If Bit 0 is a logic 0, -DTR will be inactive (logic 1). An external inverting buffer is typically used (to insure the proper polarity of -DTR) when connecting a 82C601 -DTR output to a MODEM or data set.

Bit 1: This -RTS bit determines the state of the corresponding -RTS 82C601 output pin in a fashion identical to Bit 0 (see above).

Bit 2: This bit is used to control the -OUT1 pin when Configuration Register B, bit 0, is set to 1 (the -OUT1 pin is multiplexed with -GPCS pin through Register B). If Bit 2 is set to 0, the -OUT1 pin is 1; if it is set to 1, the -OUT1 pin is 0.

Bit 3: This bit is used to control the OUT2 pin. When OUT2 = 0 (default), the serial interrupt is forced into high impedance. When OUT1 = 1 the serial interrupt output is enabled.

Note: OUT2 is an internal chip signal.

In the normal mode (no loopback), this bit is OUT2. When OUT2 = 0 (default), the serial interrupt is forced into a high impedance. When OUT2 = 1, the interrupt output is enabled.

Bit 4: The loopback bit is used for self-diagnostic purposes. If it is a lo

1. The TXD 82C601 output pin is set to a logic 1 (Marking state) and it is disconnected from the output of the Transmit Shift Register.
2. The RXD 82C601 input pin is disconnected from the Receive Shift Register.
3. The input to the Receiver Shift Register is internally connected to the output of the Transmit Shift Register.
4. All MODEM control input pins (-CTS, -DSR, -DCD, and -RI) are disconnected from the internal circuitry.
5. MODEM control output pins -DTR and -RTS are forced to their inactive state (logic 1).
6. MODEM control output -DTR is connected internally to MODEM control input -DSR, MODEM control output -RTS is internally connected to input -CTS, and MODEM Control Register (MCR) bit 2 determines the state of bit 6 of the MODEM Status Register (MSR). Bit 3 of the MCB controls bit 7 of the MSR.
7. Data which is transmitted will immediately be received, permitting the CPU to verify the data paths internal to the 82C601 and its connection to the CPU.

While operating in diagnostic loopback mode, interrupts are disabled. Interrupts are controlled by the Interrupt Enable register. Interrupts which are due to MODEM signals operate as documented, although the source is now the lower 4 bits of the MODEM Control Register rather than the MODEM input pin signals.

Bits 5, 6 and 7: These bits are set to 0.

Table 2.1 UART Interrupt Specifications (Interrupt Flag Register)

Bit 2	Bit 1	Bit 0	Priority	Type	Source	Servicing The Interrupt
0	0	1	NO	INTERRUPT	PENDING	
1	1	0	Highest	Receiver Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Read Line Status Register
1	0	0	Second	Receive Buffer Full	Receive Data	Read Receive
0	1	0	Third	Transmit Buffer Empty	Transmit Buffer	Read IFR or Write transmit buffer
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Carrier Detect	Read MODEM Status Register

2.2.9 Line Status Register (LSR)
Offset=5H, Read Only, DRAB=X

This byte-wide register supplies serial link status information to the 82C601. A Receive Line Status interrupt is caused by one of the conditions flagged by Bits 1 through 4 of this register. It is read-only. Writes to it are used at the factory for testing purposes and are not recommended. Bit definitions are as follows:

Bit 0: This Receive Buffer Full (RBF) bit is set to a logic 1 when an incoming character has been transferred from the Receive Shift Register to the Receive Buffer. Reading the Receive Buffer resets it to a logic 0.

Bit 1: This Overrun Error bit is set to a logic 1 when a new character is transferred into the Receive Buffer before the previously received character was read by the 82C601. The previously received character is lost. When the 82C601 reads the LSR, the Overrun Error bit is reset to a 0.

Bit 2: This Parity Error bit is set to a logic 1 whenever a parity error is detected (received character has a parity other than that selected). Reading the LSR resets this bit to a 0.

Bit 3: This Framing Error bit is set to a logic 1 when an incoming character has no stop bit after the last data bit or (if parity is enabled) after the parity bit. A valid stop bit is the presence of a Mark condition (logic 1) in the proper time slot after the last data bit or the parity bit. Reading the LSR resets this bit to a 0.

Bit 4: This Break Interrupt bit will be a logic 1 if a Space condition (logic 0) is present on the RXD line for an entire character time (start bit time, plus data bit times, plus parity bit time, plus stop bit time). Reading the LSR resets this bit to a 0.

Bit 5: This Transmit Buffer Empty (TBE) bit is set to a logic 1 when an outgoing character is loaded from the Transmit Buffer (TB) into the Transmit Shift Register. If the TBE interrupt is enabled, an interrupt will be generated when this bit is set. Writing a character to the TB resets this bit to a 0.

Bit 6: This Transmitter Empty (TEMT) bit will be set to a logic 1 when both the Transmit Buffer and the Transmit Shift Register are empty. When either of these two registers contains a character, this bit will be reset to a 0.

Bit 7: This bit is set to 0.

2.2.10 MODEM Status Register (MSR)
Offset=6H, Read/Write, DRAB=X

This byte-wide register holds the current value of the MODEM control lines. It also sets a bit (to a logic 1) each time one of these control lines changes state. Reading the MSR resets all of the Change bits to 0. A MODEM Status Interrupt is generated (if it is enabled) when Bit 0, 1, 2 or 3 is set to a 1. Bit definitions are:

Bit 0: This is the Clear To Send Changed bit. It is set to a 1 if the -CTS line has changed state since the last time the MSR was read.

Bit 1: This is the Data Set Ready Changed bit. It is set to a 1 if the -DSR line has changed state since the last time the MSR was read.

Bit 2: This is the Rising Edge of Ring Indicator bit. It is set to a 1 if the -RI line has changed from a logic 0 to a logic 1 since the last time the MSR was read.

Bit 3: This is the Data Carrier Detect Changed bit. It is set to a 1 if the -DCD line has changed state since the last time the MSR was read.

Bit 4: This is the Clear To Send bit. It is the complement of the -CTS pin. When in diagnostic loopback mode, this bit is identical to the RTS bit in the MODEM Control Register (MCR).

Bit 5: This is the Data Set Ready bit. It is the complement of the -DSR pin. When in diagnostic loopback mode, this bit is identical to the DTR bit in the MCR.

Bit 6: This is the Ring Indicator bit. It is the complement of the -RI pin. In diagnostic loopback mode, it is controlled by Bit 2 of the MCR.

Bit 7: This is the Data Carrier Detect bit. It is the complement of the -DCD pin. In diagnostic loopback mode, it is controlled by Bit 3 of the MCR.

2.2.11 Scratchpad Register
Offset=7H, Read/Write, DRAB=X

This byte-wide register has no effect on the UART within which it is located. It can be used for any purpose by the programmer.

2.3 Effects of Hardware Reset

The table 2.2 details the effect of a hardware RESET on the UART located in a 82C601. Note that the 82C601 has a configuration option which permits only a part of the UART to be reset when a hardware RESET is applied. This option is useful when the 82C601 will monitor a serial link and wake up the CPU upon receipt of an incoming character. Bit 7 in 82C601 Configuration Register 1 controls this option. When Bit 7 is a 0, all registers in the UART except the Receive Buffer, Transmit Buffer and the Divisor Registers (LSB and MSB) will be reset when a hardware RESET occurs. If Bit 7 is a 1, none of the registers in the UART will be reset. See the Configuration section for more details. Table 2.2 assumes that Bit 7 of the 82C601 Configuration register is a zero.

Table 2.2 Action of a Hardware Reset on the 82C601 UART

Register or Signal	Cause of Reset	Reset State
Interrupt Enable Register	Hardware RESET	All bits = logic 0
Interrupt Flag Register	Hardware RESET	Bit 0 = logic 1 Other bits = logic 0
Byte Format Register	Hardware RESET	All bits = logic 0
MODEM Control Register	Hardware RESET	All bits = logic 0
Line Status Register	Hardware RESET	Bits 5, 6 = logic 1 Other bits = logic 0
MODEM Status Register	Hardware RESET	Bits 0-3 = logic 0 Bits 4-7 = Input Signal
TXD2 and TXD1	Hardware RESET	logic 1 (high)
Receive Line Status Interrupt	Hardware RESET or Read LSR	logic 0 (low)
Receive Buffer Full Interrupt	Hardware RESET or Read RB	logic 0 (low)
Transmit Buffer Empty Interrupt	Hardware RESET or Read TB	logic 0 (low)
MODEM Status Interrupt	Hardware RESET or Read MSR	logic 0 (low)
-RTS2 and -RTS1	Hardware RESET	logic 1 (high)
-DTR2 and -DTR1	Hardware RESET	logic 1 (high)

2.4 Baud Rate Generation

The UART contains a programmable Baud Generator. The output frequency of the Baud Rate Generator is 16 X the baud rate, [(divisor # = (frequency input) ÷ (baud rate X 16)]. The output of the Baud Rate Generator drives the transmitter and receiver sections of the serial channel. Two 8-bit latches store the divisor in a 16-bit binary format. This Divisor Latch must be loaded during initialization to ensure proper operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud Counter is loaded.

Table 2.3 lists decimal divisors to use with a crystal frequency of 1.8432 MHz. The oscillator input to the chip should always be 1.8432 MHz to ensure that the timing is accurate and that the UART divisors are compatible with existing software. Using a divisor of zero is not recommended.

Table 2.3 Divisors, Baud Rates and Clock Frequencies

Divisor Baud Rate	1.8432 MHz Clock	
	Decimal Divisor for 16 X Clock	Percent Error (Note1)
50	2304	0.001
75	1536	
110	1047	
134.5	857	0.004
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.005
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	0.030
115200	1	

Note 1: The percent error for all Baud Rates, except where indicated otherwise, is 0.002%.

2.5 Serial Port Connector

The 82C601 receives and transmits TTL level signals. These signals should be buffered to achieve the desired interface. For example for RS232, 1488/1489 or 145406 type buffers can be used. The connector for the serial port is either a male 25 pin D-shell or a male 9 pin D-shell. Typically the signals are connected as shown below.

DB9	DB25	I/O	Signal
---	1	-	N/C
1	8	I	DCD
2	2	O	-TxD
—	9-19	-	N/C
3	3	I	-RxD
4	20	O	DTR
7	4	O	RTS
—	21	-	N/C
8	5	I	CTS
9	22	I	RI
6	6	I	DSR
—	23-25	-	N/C
5	7	-	Ground

3.0 PARALLEL PORT

3.1 Introduction

The Parallel Port is compatible to the IBM XT/AT Parallel Port, plus PS/2 like extended mode for bi-directional mode. When the parallel port is disabled via configuration register, all outputs are disabled, and register contents are preserved. Upon power up, the control signals are inactive. The status register reflects the status signals.

3.2 Printer Interface Accessible Registers

Table 3.1 depicts the registers and I/O ports which are accessible for the parallel printer port. These are compatible with the IBM PC parallel port. Bit definitions for each of these registers are given after the diagram. All addresses for the parallel port are offsets from the base address specified during the 82C601 configuration process.

3.2.1 Data Latch (Port A) Offset = 00H

This read/write register is located at an offset of 0H from the base address of the parallel port. Data written to this register is transmitted to the printer. Data read from this port is identical to that which was last written.

3.2.2 Printer Status Register (Port B) Offset=01H

This read-only register is located at an offset of 1H from the base address of the parallel port. Bit definitions are as follows:

Bit 7: -Busy - Printer busy. This bit reflects the state of the 82C601 -BUSY input pin. A 0 means that the printer is busy and cannot accept data. A 1 indicates that the printer is ready to accept data.

Bit 6: -ACK - Acknowledge. This bit reflects the state of the 82C601 -ACK input pin. A 0 means that the printer has received a character and is ready to accept another. A 1 means that it is still reading the last character sent or data has not been received.

TABLE 3.1 SUMMARY OF ACCESSIBLE PARALLEL PORT REGISTERS

	7	6	5	4	3	2	1	0	
XX0H	DATA								DATA LATCH (PORT A)
XX1H	BUSY	-ACK	PE	-SCLTIN	-ERROR	R	R	R	STATUS (PORT B)
2H	R	R	DIR	IRQEN	-SLCTIN	-INT	-AUTOFD	-STROBE	CONTROL(PORT C)

Note: R means Reserved

Bit 5: PE - Paper Empty. This bit reflects the state of the 82C601 PE input pin. A 1 indicates a paper end condition. A 0 indicates the presence of paper.

Bit 4: SLCT - Select. This bit reflects the state of the 82C601 SLCT input pin. A 1 means the printer is on line. A 0 means it is not selected.

Bit 3: -ERROR. This bit reflects the inverted state of the 82C601 -ERROR input pin. A 0 means that an error condition has been detected. A 1 indicates no errors.

Bits 2-0: Res

3.2.3 Printer C. ols Register (Port C)
Offset = 0..

This read/write register is located at an offset of 02H from the base address of the parallel port. Bit definitions are:

Bits 7-6: Reserved. Reset to 0.

Bit 5: Parallel Control Direction, valid in extended mode only (CR#1 <6>=1). In printer mode, the direction is always out, regardless of the state of this bit. In the extended mode, a 0 means an output/write condition. A 1 means an input/read condition.

Bit 4: IRQEN. This bit is used to enable or disable interrupts resulting from the printer -ACK signal. A 1 generates interrupts when -ACK changes from active to inactive. The CPU will be interrupted on the IRQ line specified in the 82C601 configuration RAM. A 0 means that IRQ is disabled.

Bit 3: -SLCTIN (pin 52, -SLCTIN). Used to drive the 82C601 -SLCTIN output pin . A 1 selects the printer. A 0 means the printer is not selected.

Bit 2: -INIT (pin 54, -INIT). Used to control the 82C601-INIT output pin. A 0 (active low) starts the printer (50 us pulse minimum). A 0 initializes the printer.

Bit 1: -AUTOFD (pin 55, -AUTOFD). Used to control the 82C601 -AUTOFD output pin. A 1 causes the printer to generate a line feed after each line is printed. A 0 means no autofeed.

Bit 0: -STROBE (pin 51, -STROBE). Used to control the 82C601 -STROBE output pin. A 1 in this bit generates the active low pulse (0.5 us pulse minimum) which is required to clock data into the printer. There is a 0.5 us data setup time requirement before -STROBE can be asserted. A 0 means there will be no strobe.

3.3 Hardware Reset

The hardware reset is performed by applying the logic 1 to the 82C601 RESET pin. The table below shows the value of the parallel port registers after the hardware reset.

Parallel Register	Reset Value
Data Register	Don't care
Status Register	80H
Control Register	00H

3.4 Parallel Port Connector

The parallel port connector is a DB-25 female connector. The 82C601 parallel port signals are connected directly to the parallel port connector. Typically the signals are assigned to the pins as show below:

Pin	I/O	Name
1	O	-STROBE
2-9	I/O	PD0-PD7
10	I	-ACK
11	I	BUSY
12	I	PE
13	I	SLCT
14	O	-AUTOFD
15	I	-ERROR
16	O	-INIT
17	O	-SLCTIN

3.5 About Port Assignments

There is a fallacy in the serial and parallel port assignments, that logical name such as COM1 is always at the assigned address 3F8H-3FFH, and uses IRQ4. Logical name has no bearing on the address assignment. For instance, COM1 logical name is assigned to the first serial port found by the ROM BIOS, regardless of the IRQ or address assignment. But the addresses are paired with the assigned interrupts, also there is a sequence of addresses the BIOS will search.

There are two standard serial ports, COM1 and COM2, and there are three standard parallel ports, LPT1, LPT2, and LPT3.

Historically the parallel port was always integrated with the graphics adapter card, and it was hardwired to I/O addresses 3BCH-3BFH and IRQ5, thus became LPT1. The serial ports normally resides on an multi-function adapter, along with a parallel port, and a game port. In this multi-function card, the base addresses and interrupts of the serial port and parallel ports are jumper configurable. There are four possible configurations for each serial port, and three configurations for the parallel port. For the parallel port, all three configurations are standard and fully supported by the ROM BIOS. Unlike the serial ports, only 3F8H-3FFH w/IRQ4 and 2F8H-2FFH w/IRQ3 are standard. The other two are not standard, nor supported by the ROM BIOS. Essentially they need separate device drivers.

Standard Serial Port
1. 3F8H IRQ4
2. 2F8H IRQ3

Extended Serial Port
3. 338H/3E8H/2E8H/220H IRQ4
4. 238H/2E8H/2E0H/228H IRQ3

Standard Parallel Port
1. 3BCH IRQ5
2. 378H IRQ7
3. 278H IRQ5

Note: The extended Serial Port addresses shown above are a sample of the most commonly used I/O addresses.

3.6 Other Features

In the MOTHERBOARD mode, pin 3(73) (PLCC(PFP)) defaults to -GPCS output, CR#0BH<0> is 0. -GPCS is a user definable chip select, the base address is defined in registers CR#09H and CR#0AH. A mask can also be programmed so that -GPCS can be active for a block of 2 to 16 addresses, using CR#0AH bits 7 through 5. CR#0AH<1> enables or disables the chip select, 0 = disable, 1 = enable. CR#0AH<0> allows -GPCS to be included in DBDIR decoding; that when -GPCS and -IOR are active, DBDIR will be low, assuming that -GPCS is enable (CR#0AH<1> = 1). Pin 3(73) can also be programmed to be OUT1 output from the Primary Serial Port, if CR#0BH<0> is 1. In this case, the state of pin 3(73) depends on the Modem Control Register bit 2; it becomes the complement of MCR bit 2. Some modem manufacturers use OUT1 output to control some function of the Modem, for example the software controlled reset.

3.7 Crystal Specifications

The 1.8432 MHz crystal should be: operate in the fundamental mode, have parallel resonance, 13 pF shunt capacitance load, 550 Ohm series resistance, and maximum ESR, 50 PPM tolerance.

4.0 INTEGRATED DRIVE ELECTRONICS INTERFACE

4.1 Introduction

The IDE interface allows users to utilize hard disks with embedded controller (AT and XT interface). The 82C601 provides the control signals for the IDE interface and the IDE buffers, as shown below:

-IDEENL:	Low Byte Buffer Enable(AT and XT).
-IDEENH	High Byte Buffer Enable (AT only).
-HDCS:	Hard Disk Chip Select used to access the Task File Registers decodes 1F0H-1F7H (AT) or 320H-323H (XT).
-IOCS16:	When active it indicates 16 bit I/O transfer (AT only).
-IDED7:	D7 of the IDE interface should be connected to this pin (AT only).
-HDACK:	Hard Disk DMA Acknowledge (MOTHERBOARD XT mode only).

-IDEENL becomes active when the 82C601 decodes addresses 1F0H-1F7H, 3F6H, and 3F7H in the AT mode, or 320H-323H and DMA transfers (-HDACK=0) in the XT mode. -IDEENH becomes active only when -IOCS16 is active and address range 1F0H-1F7H, and in AT mode (CR#0CH<6>=0). -IOCS16 is generated by the Hard Disk Controller when it requires a 16 bit transfer. IDED7 should be connected directly to data bit 7 of the IDE interface. The AT mode supports programmed I/O only (8 and 16 bit). XT mode supports only 8 bit DMA and 8 bit programmed I/O. The -IOCS16/-HDACK pin is multiplexed, in the AT mode it is -IOCS16, in the XT mode it is -HDACK signal.

4.2 AT/XT Modes in IDE Interface

There are 2 IDE interface modes:

AT mode: 8/16 bit programmed I/O only (no DMA). AT mode decodes addresses 1F0H-1F7H, 3F6H and 3F7H. Normal transfer is 8 bit; 16 bit transfer is performed when -IOCS16 is active and on data register (1F0H). Both -IDEENL (low buffer enable) and -IDEENH (high buffer enable) are active during 16 bit transfer. -HDCS is active whenever the 82C601 decodes programmed I/O address 1F0H-1F7H. -IDEENL is active on all AT mode addresses. On the low byte buffer, only 7 bits (D0-D6) are connected to the data bus. Bit 7 is a special case; it is sourced from the 82C601. On the IDE interface, -IDED7 is connected directly to the connector. D7 of the 82C601 provides data bit 7 to the host interface. Normally the 82C601 functions as a buffer for D7, but, when reading 3F7H, D0-D6 of the 82C601 are tri-stated and -IDEENL is enabled to transfer data bits D0-D6 from the IDE to the host; D7 should be supplied by the Floppy Disk Interface.

XT mode: 8 bit programmed I/O or DMA (no 16 bit). Normally DMA transfer is done for the data register (320H) only. During a DMA cycle (indicated by active AEN and -HDACK) -IDEENL is active, allowing the data to flow through the low byte buffer. XT mode decodes I/O address range 320H-323H.

4.3 Hard Disk Register

Below is the short summary description and bit definition of the hard disk registers. More information can be obtained from IBM AT Technical Reference.

4.3.1 Task File Registers

Data Register (1F0H, R/W)

Read and Write to sector buffer. Accessed only when Read or Write command is executed.

Error Register (1F1H, R)

This register contains the status of the last executed command.

Bit 0: Set 1 if Data Address Mark not found.
Bit 1: Set 1 if track 0 is error.
Bit 2: Set 1 if command is aborted.
Bit 3: Not used.
Bit 4: Set 1 if ID is not found.
Bit 5: Not used.
Bit 6: Set 1 if Data ECC error.
Bit 7: Set 1 if bad block detect.

Write Compensation Register (1F1H, W)

This register contains the starting cylinder value divided by 4.

Sector Count Register (1F2H, R/W)

This register contains the number of sectors during a Verify, Read, Write or Format command. Note that a 0 value means 256 sector transfer.

Sector Number Register (1F3H, R/W)

This register contains the target's logical sector number of Read, Write and Verify command.

Cylinder Number Register (R/W)
1F4H = Low, 1F5H = High

These registers contain LSB and MSB of the first cylinder number where the disk is to be accessed for Read, Write, Seek and Verify command.

Drive/Head Register (1F6H, R/W)

Bit 7,5: Set to 1
Bit 6: Set to 0
Bit 4: Drive select. Primary = 0, Secondary = 1
Bit 3-0: 4 bit binary represents the head number (bit3:MSB and bit0:LSB)

Status Register (1F7H, R)

This register contains the status of the drive:

Bit 7: Set to 1 if the drive is busy
Bit 6: Set to 1 if the drive is ready to accept command.
Bit 5: Set to 1 if write fault condition occurred.
Bit 4: Set to 1 if seek command is completed.
Bit 3: Set to 1 if drive is ready to transfer data.
Bit 2: Set to 1 if data correction is successful.
Bit 1: Set to 1 if index mark is detected.
Bit 0: Set to 1 if error occur from last command.

Command Register (1F7H, W)

This register contains command op code for fixed disk operation.

4.3.2 Other Registers

Digital Input Register Definition (3F7H, R)

bit 7: Diskette Change, Diskette interface status (FDC)
bit 6: Write Gate (HDC)
bit 5: Head Select 3/Reduced Write Current (HDC)
bit 4: Head Select 2 (HDC)
bit 3: Head Select 1 (HDC)
bit 2: Head Select 0 (HDC)
bit 1: Drive Select 1 (HDC)
bit 0: Drive Select 0 (HDC)

Fixed Disk Register (3F6H, W)

bits 7-4: Not Used
bit 3: HEAD3 N
bit 2: RESE
0 = Normal operation, default
1 = Generate reset to HDC
bit 1: -IRQEN
0 = Enabled interrupt
1 = Disable interrupt, default
bit 0: Reserved

5.0 THE 82C601 CONFIGURATION (MOTHERBOARD MODE ONLY)

5.1 Introduction

A significant portion of the 82C601 circuitry is used for configuration, all of which can be performed under software control. This permits user-friendly (probably menu-driven) 82C601 configuration using setup utilities provided with the card or system containing the 82C601. DIP switches and jumpers can thus be eliminated meaning that it should no longer be necessary to open the chassis to change the configuration of a peripheral.

Since the 82C601 is software configured, a setup program must be run any time configuration is changed. This process entails placing the 82C601 in configuration mode and setting the on-chip configuration registers.

5.2 Configuration Sequence

In order to setup or change the configuration of the 82C601, two consecutive I/O addresses (one even and one odd; these should not conflict with any existing devices) are used to select and access the internal configuration registers. The configuration sequence is intentionally complicated to prevent accidental changes to the 82C601 configuration by an errant program. Any deviation from the sequence described below will cause the configuration state machine to return to its initial idle state.

By IBM PC convention, I/O addresses 3F8-3FFH and 28F-2FFH are reserved for COM1 and COM2 respectively. The Interrupt Flag Register (IFR), located by default at 2FAH or 3FAH in each 82C601, is normally read-only. Writes to these locations are tolerated by the 82C601, and they should present no problem for resident NS16450 or INS8250A UARTs. Note that there are special considerations when using more than one 82C601 in a single system.

The configuration sequence is divided into three steps:

1) Entering the configuration mode
2) Configuring the 82C601
3) Escaping the configuration mode.

The description of each step with examples is as follows:

5.2.1 Getting in/out of the configuration mode

Getting into the configuration mode requires the correct order of 5 consecutive values and addresses to be written into I/O addresses 2FAH and 3FAH, as shown below. Steps 4 and 5 determine the address for the Configuration Register Index and Data pair. The lower address is the CRI, the higher address is the CRD (CRD = CRI + 1). The CRI, CRD pair should be selected carefully so that they do not interfere with any other addresses in the system. The CRI address can be calculated by multiplying the value written in step 4 by 4. The value written in step 5 is the one's complement of the value written in step 4. In the example below, the CRI was chosen to be 390H which corresponds to a value of E4H to be written into step 4.

This results to 1BH, one's complement of E4H, being written to 2FAH in step 5. To exit the configuration mode, write any value into Configuration Register #0FH.

To get into configuration mode:

1) Write 55H to 2FAH.
2) Write AAH to 3FAH.
3) Write 36H to 3FAH.
4) Write E4H to 3FAH (see above).
5) Write 1BH to 2FAH (see above).

***** In configuration mode *****

To exit from configuration mode:

7) Write 0FH to CR#0FH.

Example:
(the CRI is 390H, CR#0H is set to AEH)

```
;step 1
MOV     DX,2FAH     ;I/O address 2FAH
MOV     AL,55H
OUT     DX,AL       ;write 55H into 2FAH
;step2
MOV     AL,0AAH
MOV     DX,3FAH     ;I/O address 3FAH
OUT     DX,AL       ;write AAH to 3FAH
;step3
MOV     AL,36H
OUT     DX,AL       ;write 36H into 3FAH
;step4
MOV     AL,0E4H     ;390H/4 = E4H
OUT     DX,AL       ;write E4H to 3FAH
;step 5
MOV     AL,1BH      ;1BH is 1s complement of
                      0E4H
MOV     DX,2FAH
OUT     DX,AL       ;write 1BH to 2FAH

;*****Now we are in the configuration mode*****

;Set Config. Reg. #0H to AEH
MOV     DX,390H     ;set CRI to 390H
MOV     AL,00H      ;CR#0H
OUT     DX,AL
INC     DX          ;Config. Reg. Data = 391H
MOV     AL,0AEH     ;Valid config. OSC on w/
                      PWRGD, Enable all
OUT     DX,AL       ;write 0AEH to CRD

;Exit from Configuration Mode

DEC     DX          ;set DX to CRI
MOV     AL,0FH      ;CR#0FH
OUT     DX,AL
INC     DX          ;set DX to CRD
OUT     DX,AL       ;Exit Configuration Mode
```

5.3 Configuration Register Description

There are 16 configuration registers in the 82C601 which must be initialized. Settings are retained as long as standby power is maintained.

These registers are not affected by the RESET signal and are set to their default state only upon power up. Table 5.1 depicts the configuration registers in the 82C601 with the default values upon power up. The definitions for each of the bits in the 82C601 configuration registers are shown below.

Upon power up the configuration registers are set to the default values, control signals are inactive, status registers reflect the status of the input pins, other registers are cleared to 00H, and unused bits are cleared to 0s. All the control signals and the register contents are preserved as long as power is maintained.

The default values upon power up:

CR#00H = 0EH	CR#08H = ECH
CR#01H = 00H	CR#09H = XXH
CR#02H = 08H	CR#0AH = 00H
CR#03H = XXH	CR#0BH = 00H
CR#04H = FEH	CR#0CH = 00H
CR#05H = BEH	CR#0DH = XXH
CR#06H = 9EH	CR#0EH = 00H
CR#07H = XXH	CR#0FH = N/A

Configuration Register 00H (R/W)

This read/write register is located at CRI off-set 00H.
Bit definitions are as follows:

Bit 7: Valid Configuration Indication.
This bit indicates that a valid configuration cycle has taken place. The configuration software should set this bit to 1 after it has initialized the required configuration registers.

VALUE FUNCTION

0 Invalid Configuration-Default on power-up.
Indicates that power has been applied to the 82C601 but the configuration registers have not yet been fully initialized. A reset from the RESET pin has no effect on this bit.

1 Valid Configuration
Indicates that the configuration software has initialized all necessary configuration registers since the last time power was applied to the 82C601.

Bits 6-5: Serial Port Oscillator Enable.

VALUE FUNCTION

b6 b5
0 0 Oscillator always ON, default

0 1 Oscillator is ON when PWRGD is active, otherwise it is OFF (tri-state)

1 0 Oscillator is ON when PWRGD is active, otherwise it is OFF (tri-state)

1 1 Oscillator always OFF

VALUE DESCRIPTION

0 Oscillator ON, BR Generator Clock ENABLED
In this state the oscillator and Baud Rate Generator Clock are always enabled and are not shut off due to removal of PWRGD (PWRGD pin becoming inactive). The presence of a power supply other than a (low capacity) battery is assumed. This is due to the fact that serial port operation (in particular the oscillator) consumes more power than many of the other 82C601 circuits.

1 Oscillator ON, BR Generator Clock ENABLED
In this state, the oscillator and BR Generator Clock are ON and ENABLED respectively as long as the PWRGD pin is active. When PWRGD becomes inactive, these two are shut down.

2 Oscillator ON, BR Generator Clock DISABLED
In this state the oscillator is ON as long as the PWRGD pin is active. When PWRGD becomes inactive, the oscillator is shut off. The BR Generator Clock is always disabled.

3 Oscillator OFF, BR Generator Clock DISABLED

Bit 4: Reserved (read only).

Bit 3: Parallel Port Enable; Read/Write. A 1 in this bit enables the Parallel Port. The default is enabled upon power up.

Bit 2: Secondary Serial Port Enable
0 = Disabled.
1 = Enabled, default upon power up.

Bit 1: Primary Serial Port Enable.
0 = Disabled.
1 = Enabled, default upon power up.

Bit 1: Reserved

Configuration Register 01H (R/W)

This read/write register is located at CRI offset 01H. Bit definitions are as follows:

Bit 7: Reset Control. This bit determines the manner in which the RESET pin affects the serial port. Default is normal RESET.

VALUE FUNCTION

0 Normal RESET.
The 82C601 RESET input will cause a reset of all serial port registers to the default values except for the Receive Buffer, Transmit Buffer and Divisor Registers.

1 Restricted RESET.
The RESET input will not reset the serial ports. This is used in applications where the 82C601 remains powered from an external supply while power to the remainder of the system is shut off. When the system power is restored, (most likely due to an interrupt when a character is received) it is desirable to have the state of the serial port remain unchanged.

Bit 6: Printer Port Operation. This bit defaults to 0.

VALUE FUNCTION

0 Normal, for printer only.
In this mode, the data read from the Parallel Data Latch register is identical to that which was last written.

1 Bi-directional or Extended mode.
In this mode, write data to Parallel Data Latch register will latch the data and be sent to the parallel connector when the DIR bit (bit 5 of Parallel Control Register) is set to Write direction. The DIR bit should be set to Read direction in order to read the connector data. Otherwise the latched data is read.

Bit 5: Forces UART -CTS1 active. A 1 in this bit forces the 82C601 internal -CTS1 signal low. Default is not forced and the output is dependent on the programmed Modem Control Register valve.

Bit 4: Forces UART -DSR1 active. A 1 in this bit forces the 82C601 internal -DSR1 signal low. Default is not forced and the output is dependent on the programmed Modem Control Register valve.

Bit 3: Forces UART -DCD1 active. A 1 in this bit forces the 82C601 internal -DCD1 signal low. Default is not forced and the output is dependent on the programmed Modem Control Register valve.

Bit 2: Forces -CTS2 active.

Bit 1: Forces -DSR2 active.

Bit 0: Forces -DCD2 active.
A 1 in any of bits 0-5 will force the appropriate inputs to active (low). The default is not forced, that is, the output is dependent on the programmed Modem Control register value.

Configuration Register 02H (R/W)

This read/write register is located at CRI offset 02H. Bit definitions are as follows:

Bit 7: Reserved = 0 (read/write).

Bit 6: Primary UART Clock Divider. Divides UART clock by 2 or 4.

VALUE	FUNCTION
0	Divide by 2 (default)
1	Divide by 4

Bit 5: Primary UART Receive Clock Select.

VALUE	FUNCTION
0	Use baud rate generator output (default)
1	Use divider output (see bit 6)

Bit 4: Primary UART Transmit Clock Select.

VALUE	FUNCTION
0	Use baud rate generator output (default)
1	Use divider output (see bit 6)

Bit 3: 8250 or 16450 mode.
0 = 8250 mode.
1 = 16450 mode, default.

The difference between 8250 and 16450 mode is when there are multiple interrupts pending. In 8250 mode the 82C601 will bring the INTR line low momentarily after each read of the interrupt status. However, after the last interrupt the INTR will remain inactive. In the 16450 mode, no low pulse will be generated. The INTR will become inactive (low) after the last interrupt status is read.

Bit 2: Secondary Serial Port clock divider.
0 = Divide by 2, default.
1 = Divide by 4.

Bit 1: Secondary Serial Port Receive clock.
0 = Baud Rate Generator, default.
1 = Divider output (see bit 2).

Bit 0: Secondary Serial Port Transmit clock.
0 = Baud Rate Generator, default.
1 = Divider output (see bit 2).

Configuration Register 03H Reserved

Configuration Register 04H (R/W)
(UART base address)

This read/write register holds the base address of the UART. It is located at CRI offset 04H. The high order seven bits in this one byte register are compared with SAD<09:03>when the 82C601 is in normal operating mode to determine if the UART is being addressed. Nominal settings are 2F8H (COM2) or 3F8H (COM1). Default upon power up is FEH: address 3F8H (COM1).

Bits 7-1: The MSB of the Primary Serial Port Address (bits 9-3)

Bit 0: Reserved = 0 (If read will be zero)
Default upon power up is FE4: address 3F8H (COM1).

Configuration Register 05H (R/W)

b7-b1: The MSB of the Secondary Serial Port Address (bits 9-3)
b0: Reserved = 0.
Default upon power up is BEH: address 2F8F (COM2).

Configuration Register 06H (R/W)
(Parallel base address)

b7-b0: The 8 MSB of the Parallel Port.
Default upon power up is 9EH: address 278H (LPTC).

This read/write register holds the base address of the parallel port. It is located at CRI offset 06H. The eight bits in it are compared with SAD<09:02> when the 82C601 is in normal operating mode to determine if the Parallel Port is being addressed. Nominal settings are 278H (LPTC) or 378H (LPTB). Default is 278H. (LPTC is assumed to be on the monochrome adapter).

Configuration Register 07H: Reserved

Configuration Register #08H (R/W)
Interrupt Request Source.

Bits 7-6: INTR1 Source.

b7	b6	
0	0	Disabled, tri-stated.
0	1	Disabled, tri-stated.
1	0	Primary Serial Port.
1	1	Secondary Serial Port, default.

Bits 5-4: INTR2 Source.

b5	b4	
0	0	Disabled, tri-stated.
0	1	Disabled, tri-stated.
1	0	Primary Serial Port, default.
1	1	Secondary Serial Port.

Bit 3-2: INTR3 Source.

b3	b2	
0	0	Disabled, tri-stated.
0	1	Disabled, tri-stated.
1	0	Primary Serial Port
1	1	Parallel Port, default.

Bit 2: Secondary Serial Port clock divider.
0 = Divide by 2, default.
1 = Divide by 4.

Bit 1: Secondary Serial Port Receive clock.
0 = Baud Rate Generator, default.
1 = Divider output (see bit 2).

Bit 0: Secondary Serial Port Transmit clock.
0 = Baud Rate Generator, default.
1 = Divider output (see bit 2).

Configuration Register 09H (R/W)
(General Purpose Chip Select address)

This read/write register is located at CRI offset 09H. Bit definitions are as follows:

Bits 7-0: A9-A2 Address Decode

Configuration Register 0AH (R/W)

This read/write register is located at CRI offset 0AH. Bit definitions are as follows

Bits 7-5:
-GPCS mask for address bit 3 to bit 1.

VALUE FUNCTION

0 No mask

1 Mask (not used in decoding)

Bit 4: Reserved.

Bit 3: -GPCS A1 address decode

Bit 2: -IDEENL Buffer Enable

VALUE FUNCTION

0 Disabled (default)

1 Enabled. -IDEENL qualifies DBDIR

Bit 1: -GPCS Enable

VALUE FUNCTION

0 Disabled (default). -GPCS is high.

1 Enable -GPCS output.

Bit 0: -GPCS Buffer Enable

VALUE FUNCTION

0 Disabled (default)

1 Enabled. -GPCS qualifies BDIR

Configuration Register 0BH (R/W)
Interrupt Polarity Select and Power Down.

This read/write register is located at CRI offset 0BH. Bit definitions are as follows:

Bit 7: INTR4 Polarity Select.
0 = Active High, default.
1 = Active low, tri-stated when inactive.

Bit 6: INTR3 Polarity Select.
0 = Active High, default.
1 = Active low, tri-stated when inactive.

Bit 5: INTR2 Polarity Select.
0 = Active High, Default.
1 = Active Low, tri-stated when inactive.

Bit 4: INTR1 Polarity Select.
0 = Active High, default.
1 = Active Low, tri-stated when inactive.

Bit 3: Primary Serial Port Power Down

VALUE FUNCTION

0 Normal Mode (default)

1 Power Down Mode

Bit 2: Secondary Serial Port Power Down.
0 = Normal mode, default.
1 = Power Down mode.
All outputs are tri-stated, all inputs are disabled.
Outputs: TxD, -RTS, -DTR.
Inputs: RxD, -CTS, -DSR, -DCD, -RI.

Bit 1: Parallel Port Power Down

VALUE FUNCTION

0 Normal Mode (default)

1 Power Down Mode.
All outputs (PD0-7, -STROBE, -SLCTIN, -INT, -AUTOFD) are tri-stated.
All inputs (-ACK, BUSY, PE, SLCT, -ERROR) are disabled.

Bit 0: -GPCS/OUT1 Pin Function Select

VALUE FUNCTION

0 -GPCS is selected as output pin. (default)

1 OUT1 of UART (MCR) is selected as output pin.

Configuration Register 0CH (R/W)

This read/write register is located at CRI offset 0CH. Bit definitions are as follows:

Bit 7: IDE Enable

VALUE FUNCTION

0 IDE disabled, default.
-HDCS, -IDEENL, -IDEENH are always disabled (high).

1 IDE Enabled
-HDCS, -IDEENL are enabled, and will be active when the correct addresses are selected.
-IDEENH depends on the XT/AT mode bit and the -IOCS16 input.

Bit 6: IDE AT/XT Select

VALUE FUNCTION

0 IDE AT interface (default)
8/16 bit programmed I/O transfers.
-IDEENL is active during I/O 3F6H, 3F7H, 1F0H -1F7H. -IDEENH is active during programmed I/O 1F0H-1F7H and -HDCS is active during PIO 3F0H-3F7H.

1 IDE XT interface. 8 bit DMA and PIO transfers.
-IDEENL is active during PIO 320H-323H or DMA (-HDACK active). -HDCS is active only during programmed I/O (PIO) 320H-323H.

Bit 5: -FDCS Enable

VALUE FUNCTION

0 -FDCS Disabled, default.

Note: The FDC must also be powered down.

1 -FDCS Enabled
Floppy disk chip select is active for I/O address 3F0H-3F7H.

Bit 4: -FDCS Buffer Enable

VALUE FUNCTION

0 = -FDCS Buffer Disabled, default.
1 = -FDCS Buffer Enabled, -FDCS qualified DBDIR.

Bit 3: -RTCCS Enable

VALUE FUNCTION

0 -RTCCS Disabled (default)

1 -RTCCS Enabled.
-RTCCS is active for I/O 70H and 71H.

Bit 2: -RTCCS Buffer Enable

VALUE FUNCTION

0 -RTCCS Buffer Disabled (default)

1 -RTCCS Enabled. -RTCCS qualifies DBDIR.

Bit 1,0: Reserved (Read/Write)

Configuration Register 0DH (R/W)
Reserved = 0

Configuration Register 0EH (R/W)

This read/write register is located at CRI offset 0EH. Bit definitions are as follows:

Bit 7: Reserved.

Bit 6: Primary Serial Port Test enabled.

VALUE FUNCTION

0 Normal mode. Test disabled (default)

1 Test enabled. TXD1 outputs the Rx clock.

Bit 5: Secondary Serial Port Test Enable.
0 = Normal mode, Test Disabled, default.
1 = Test Enabled, TxD2 outputs the Rx clock.

Bit 4-0: Reserved = 0

Configuration Register 0FH (R)

This register contains the Configuration Register Index address divided by 4.

Configuration Register 0FH (W)

Writing any value into this register will bring the 82C601 out of configuration mode.

Configuration Register Summary

	b7	b6	b5	b4	b3	b2	b1	b0		DEFAULT
CR#00H	VC	SP OSC ENABLE		RSVD	PP	S2	S1	RSVD	R/W	0EH
CR#01H	RE	PP	S1 CONFIG			S2 CONFIG				00H
CR#02H	RSVD=0	S1	R1	T1	MS	S2	R2	T2	R/W	08H
CR#03H	NOT USED									
CR#04H	PSA9	PSA8	PSA7	PSA6	PSA5	PSA4	PSA3	RSVD=0	R/W	0FEH
CR#05H	SSA9	SSA8	SSA7	SSA6	SSA5	SSA4	SSA3	RSVD=0	R/W	BEH
CR#06H	PPA9	PPA8	PPA7	PPA6	PPA5	PPA4	PPA3	PPA2	R/W	9EH
CR#07H	NOT USED									
CR#08H	INTR1 SOURCE		INTR2 SOURCE		INTR3 SOURCE		INTR4 SOURCE		R/W	ECH
CR#09H	GPA9	GPA8	GPA7	GPA6	GPA5	GPA4	GPA3	GPA2	R/W	XXH
CR#0AH	MASK3	MASK2	MASK1	RSVD	GPA1	IDEBEN	GPEN	GPBEN	R/W	00H
CR#0BH	INT4PS	INT3PS	INT2PS	INT1PS	PSPD	SSPD	PPPD	G/OSEL	R/W	00H
CR#0CH	IDEEN	IDESEL	FDCSEN	FDCBEN	RTCSEN	RTCBEN	RSVD=0	RSVD=0	R/W	00H
CR#0DH	NOT USED									
CR#0EH	RSVD	S1TEST	S2TEST	RSVD=0	RSVD=0	RSVD=0	RSVD=0	RSVD=0	R/W	00H
CR#0FH	CONFIGURATION REGISTER INDEX								R/W	XXH

TABLE 5.1

6.0 82C601 POWER MANAGEMENT (IN MOTHERBOARD APPLICATION)

6.1 Introduction

Power management functions are achieved using PWRGD pin (hardware) and Configuration Register bits (software). The 82C601 configurations and register data can be retained during sleep mode with the minimum current drain. This makes the 82C601 ideal for laptop environments. Each port of the 82C601 can also be individually disabled or powered down through configuration registers. This feature enhances the 82C601's flexibility in system integration. The section below discusses the power management of the 82C601.

6.2 Power Management Application

There are three typical operating modes for any system.

1) Active mode
2) Sleep mode
3) Power Down mode.

Active mode:

In this mode, the 82C601 will be powered by a power supply (through AC outlet) or in a laptop by a main battery (NiCd). The configuration registers will be initialized by the System BIOS. In Active mode, software (BIOS) can power off selected resources when needed to reduce total power consumption.

Sleep mode:

In a Laptop application, the power source is the main battery which can last from 4-12 hours. To save battery energy, the system should be put in sleep mode which draws a minimum current when it is not used. The 82C601 supports this sleep mode feature through PWRGD pin and bits 6 and 5 of configuration register 0H (CR#0H<6,5>). Below is a detailed description of these bit functions.

b6,b5: Serial Port & Floppy Oscillator Enable.

0	0	Oscillator always ON regardless of PWRGD, default.
0	1	Oscillator is ON when PWRGD is high,otherwise it is OFF (tri-state)
1	0	Oscillator is ON when PWRGD is high, otherwise it is OFF (tri-state).
1	1	Oscillator is always OFF.

To implement the sleep mode, the CR#0H<6,5> should be programmed as 0,1 or 1,0. This turns off the oscillator and minimizes the current drawn by the serial and floppy ports. The PWRGD signal is controlled by user designed sleep mode circuitry. When the system is put in the sleep mode, the sleep mode circuitry will assert PWRGD. The 82C601 isolates itself from the rest of the system; all outputs are tri-stated, all inputs are disabled and all commands are ignored until the PWRGD is restored to the active state (wake up). This is why CRD is set to 0,1 or 1,0.

Power Down mode

In this mode, the power is completely removed from the system. The programmed configuration register data will not be retained. This should not be an issue since the configuration registers will be restored by the system BIOS.

Note: In any mode, the 82C601 should not be powered by the RTC backup battery (Lithium).

6.3 Enabled and Power Down Register Values

This section summarizes the Enabled/Disabled and Power Up/Down bits for each port.

Serial Port 1

CR#00H<1> = 0	Disabled
CR#00H<1> = 1	Enable (default)
CR#0BH<3> = 0	Power Up (default)
CR#0BH<3> = 1	Power Down.

Serial Port 2

CR#00H<2> = 0	Disabled
CR#00H<2> = 1	Enabled (default)
CR#0BH<2> = 0	Power Up (default)
CR#0BH<2> = 1	Power Down.

Parallel Port

CR#00H<3> = 0	Disabled
CR#00H<3> = 1	Enabled (default)
CR#0BH<1> = 0	Power Up (default)
CR#0BH<1> = 1	Power Down.

IDE port

CR#0CH<7> = 0	Disabled (default)
CR#0CH<7> = 1	Enabled

RTCCS (Real Time Clock Chip Select)

CR#0CH<3> = 0	Disabled (default)
CR#0CH<3> = 1	Enabled

GPCS (General Purpose Chip Select)

CR#0AH<1> = 0	Disabled (default)
CR#0AH<1> = 1	Enabled

FDCS

CR#0C<5> = 0	Disabled (default)
CR#0C<5> = 1	Enabled

7.0 REAL TIME CLOCK CHIP SELECT (-RTCCS) AND GENERAL PURPOSE CHIP SELECT (-GPCS)

7.1 Introduction

The 82C601 provides the Real Time Clock Chip Select (-RTCCS) which is decoded at I/O addresses 70H and 71H and the General Purpose Chip Select (-GPCS) whose address is programmable. The following section describes the application of these two signals.

7.2 The 82C601 RTC Application

The typical Real Time Clock circuit is shown in Figure 8.1.

7.3 The 82c601 Game Port Application (Adapter Mode Only)

The typical game port circuit is shown in Figure 8.4.

bit #	Name	Description
7	BTN7	Fire button 4
6	BTN6	Fire button 3
5	BTN5	Fire button 2
4	BTN4	Fire button 1
3	POS3	Joystick 4 position
2	POS3	Joystick 3 position
1	POS3	Joystick 2 position
0	POS3	Joystick 1 position

8.0 PC/AT DESIGN APPLICATION

8.1 Introduction

This section describes the 82C601 in a PC/AT MOTHERBOARD application. The complete serial port, parallel port, floppy disk port and IDE interface can be embedded in the MOTHERBOARD with minimal board space and some cost savings. Figure 8.1 shows a typical MOTHERBOARD application of the 82C601.

8.2 I/O Address Map for the PC/AT

Serial Port

Below is a table of standard PC/AT serial port addresses and the corresponding interrupts.

Physical Address	Interrupt	Logical name
3F8H	IRQ4	COM1
2F8H	IRQ3	COM2
338H / 3E8H 2E8H / 220H	IRQ4	COM3
238H / 2E8H 2E0H / 228H	IRQ3	COM4

Note that the logical name has no bearing on the address assignment. For instance, COM1 logical name is assigned to the first serial port found by the ROM BIOS, regardless of the IRQ and address assignment. However, the address is paired with the assigned interrupt. Also, there is a sequence of the addresses the BIOS will search for.

By default, the 82C601 serial port is set at the 3F8H address, and the interrupt should be hard wired to the IRQ4.

Parallel Port

Physical Address	Interrupt	Logical name
3BCH	IRQ5	LPTA
378H	IRQ7	LPTB
278H	IRQ5	LPTC

Note: The logical name has no bearing on the address assignment. For instance, LPT1 logical name is assigned to the first serail port found by the ROM BIOS, regardless of the IRQ and address assignment. However, the address is paired with the assigned interrupt. Also, there is a sequence of the addresses the BIOS will search for.

The IBM PC/AT allows installation of up to 3 parallel ports. These ports have logical names: LPTA, LPTB, LPTC. The printer port on the Monochrome/Printer Adaptor which is addressed at 3BCH will be LPTA when it is installed, then the LPTC (278H) on 82C601 (if configured) will be LPTC.

By default, the 82C601 parallel port is set at 278H address, and the interrupt should be hard wired to IRQ5.

IDE Interface

The 82C601 integrates the complete IDE interface into a single chip. The 82C601 IDE signals connect directly to the IDE connector. Two transceivers whose direction signals are controlled by -IDEENL and -IDEENH are required for the low byte and the high byte data.

PC/AT Task File Registers

I/O Address	Type Access	Description
1F0H	R/W	Data Register
1F1H	R	Error Register
	W	Write Precomp.
1F2H	R/W	Sector Count
1F3H	R/W	Sector Number
1F4H	R/W	Cylinder Low
1F5H	R/W	Cylinder High
1F6H	R/W	Drive/Head
1F7H	R	Status Register
	W	Command Reg.

PC/AT Alternate Registers

I/O Address	Type Access	Description
3F6H	W	Fixed Disk
3F7H	R	Digital Input

The description of these registers can be found in the IDE interface section.

ABSOLUTE MAXIMUM RATINGS:

Symbol	Min	Max	Unit
Supply Voltage (Vcc)	3.0	7.0	Volts
Supply Current (Icc)	10.0	40.0	mA
Input Voltage (Vi)	-0.5	5.5	Volts
Operating Temperature (Ta)	0	70	C
Storage Temperature (Tstg)	-40	125	C

DC CHARACTERISTICS:

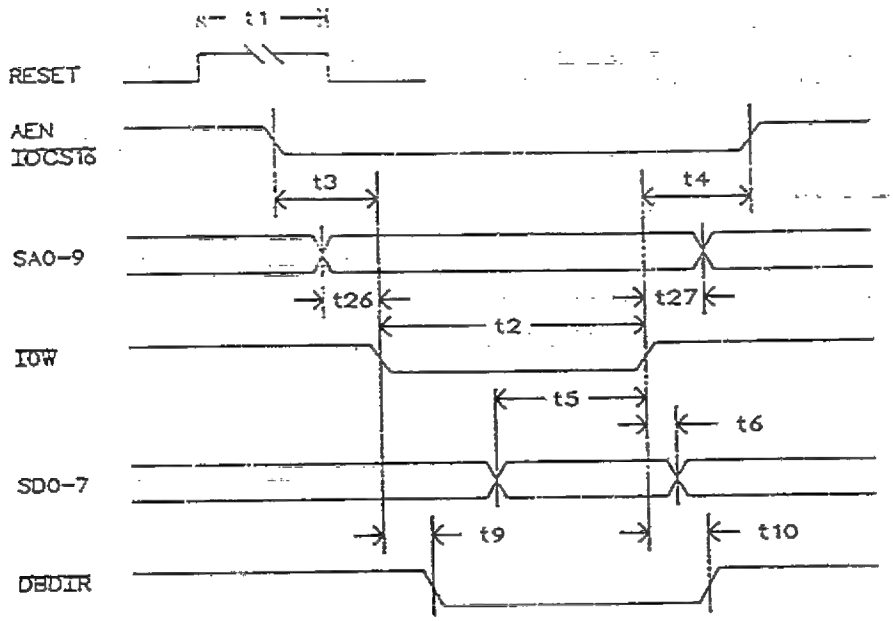
Type	Symbol	Min	Typ	Max	Unit	Test Condition
	Vcc	4.5	5.0	5.5	V	
OL	Iol	4.0			mA	Vol_max=0.4V
	Ioh	-1.0			mA	Voh_min=2.4V
O	Iol	8.0			mA	Vol_max=0.4V
	Ioh	-1.0			mA	Voh_min=2.4V
OH	Iol	16			mA	Vol_max-0.5V
	Ioh	-200			uA	Voh_min=2.4V
T	Iol	24			mA	Vol_max=0.5V
OC	Ioh	-8			mA	Voh_min=2.4V
	Iil			-20	uA	Vcc_max, Vil=0.4, all inputs
	Iih			20	uA	Vcc_max, Vih=2.7V, all inputs
	Vil			0.8	V	All inputs
	Vih	2.0			V	
	Vol			0.4	V	Iol_max, Vcc_min, Vil_max, Vih=2V
	Voh	2.4			V	Vcc_min, Ioh_max, Vil=0.5V, Vih=2V
	Istby			50	uA	Standby current without clocks, @ Vcc_min, PWRGD active

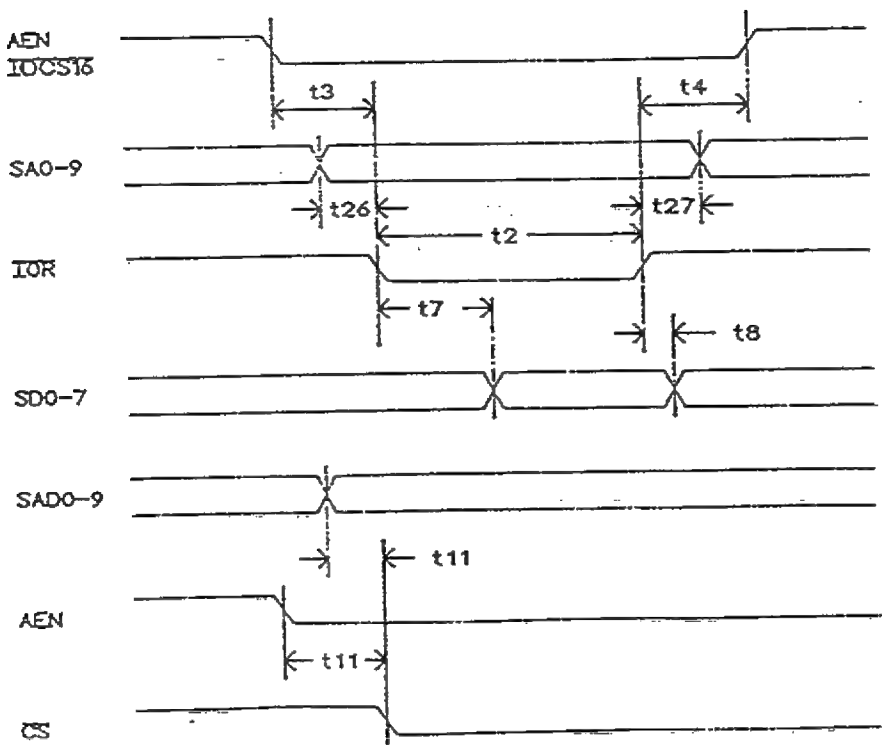
Note:
- I = TTL Input
- IS = Schmitt Trigger input
- O = TTL output
- OH = High current TTL output
- OC = Open Drain
- OL = Low current open drain output
- T = Tri-state TTL output, 24 mA

AC CHARACTERISTICS:

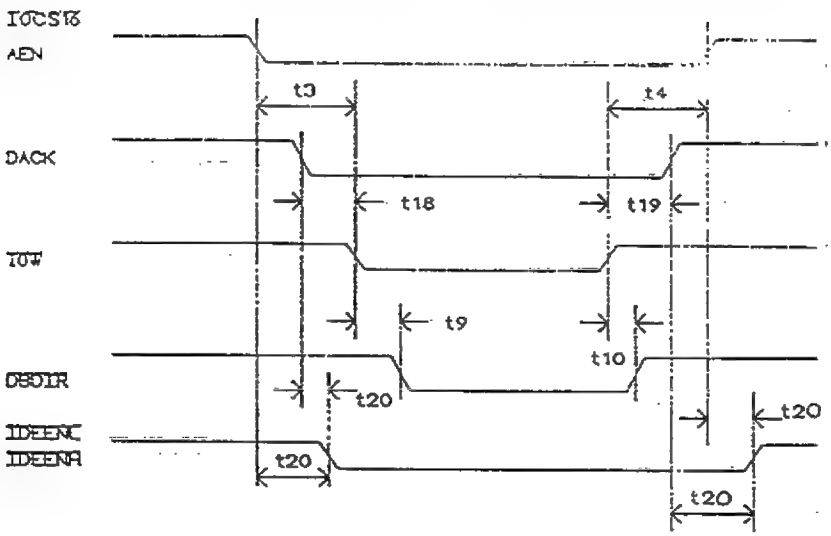
Sym	Description	Min	Max	Unit
Host Interface Timing				
t1	RESET width	1		us
t2	-IOR, -IOW width	150		ns
t3	AEN, -IOCS16 setup time to -IOR, -IOW	40		ns
t4	AEN, -IOCS16 hold time from -IOR, -IOW	10		ns
t26	SA setup time to -IOR, -IOW	40		ns
t27	SA hold time from -IOR, -IOW	10		ns
t5	SD setup time to -IOW	40		ns
t6	SD hold time from -IOW	10		ns
t7	SDdelay from -IOR	60		ns
t8	SD hold time from -IOR	0	40	ns
t9	DBDIR active delay from -IOR, -IOW		40	ns
t10	DBDIR inactive delay from -IOR, -IOW		80	ns
t11	-CS delays from AEN, SA		40	ns
Parallel Port Timing				
t12	PD, -INIT, -STROBE, -AUTOFD, -SLCTIN delay from SD		100	ns
t13	INTR delay from ACK		60	ns
IDE Interface Timing				
t14	-IDEENL, -IDEENH delay from AEN, -IOCS16		40	ns
t15	-IDEENL, -IDEENH delay from SA		40	ns
t16	IDED7 to SD7 delay (read cycle)		60	ns
t17	SD7 to IDED7 delay (write cycle)		40	ns
DMA Interface Timing				
t18	-DACK setup time to -IOR, -IOW	40		ns
t19	-DACK hold time from -IOR, -IOW	40		ns
t20	-DACK, AEN, -IOCS16 to -IDEENLL, -IDEENH delay		40	ns
Serial Port Timing				
t21	-LOW to -RTS, -DTR, -OUT1 delay		100	ns
t22	-IOW to INTR3-state delay	10	100	ns
t23	INTR active elay from -CTS, -DSR, -DCD		100	ns
t24	INTR inactive delay from -IOR		100	ns
t25	INTR inactive delay from -IOW		100	ns

HOST INTERFACE TIMING

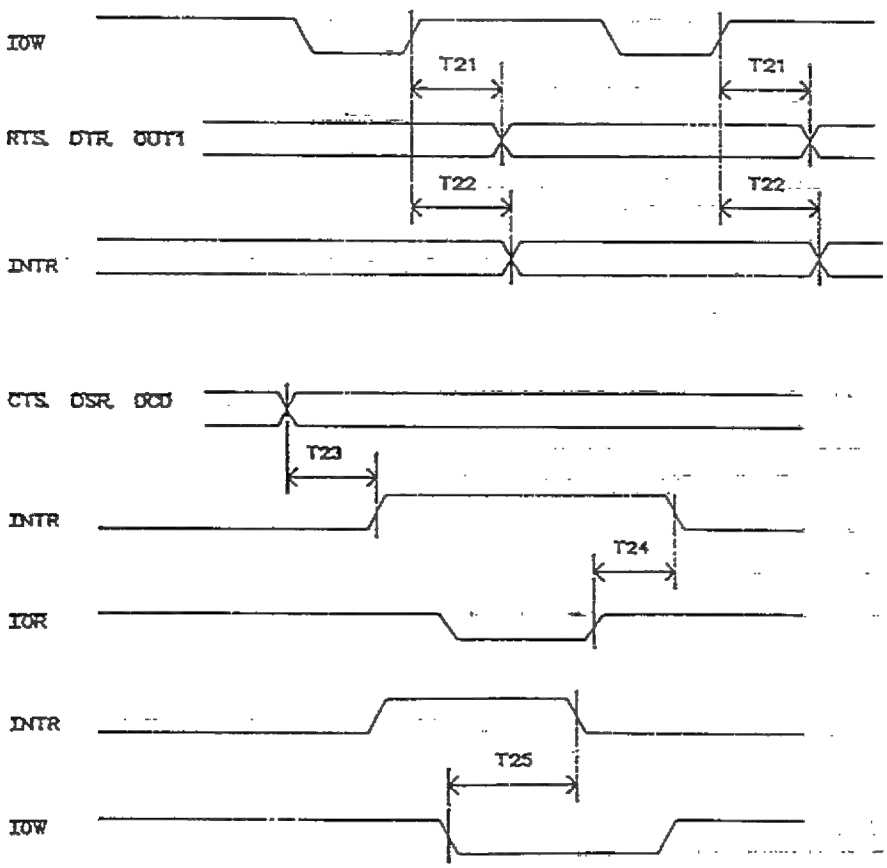




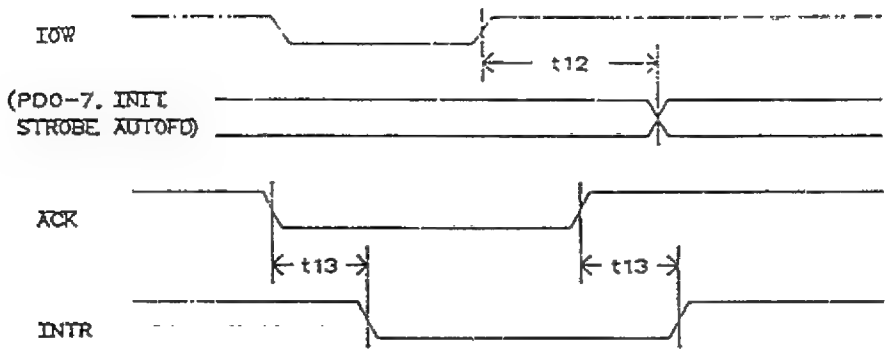
DMA TIMING



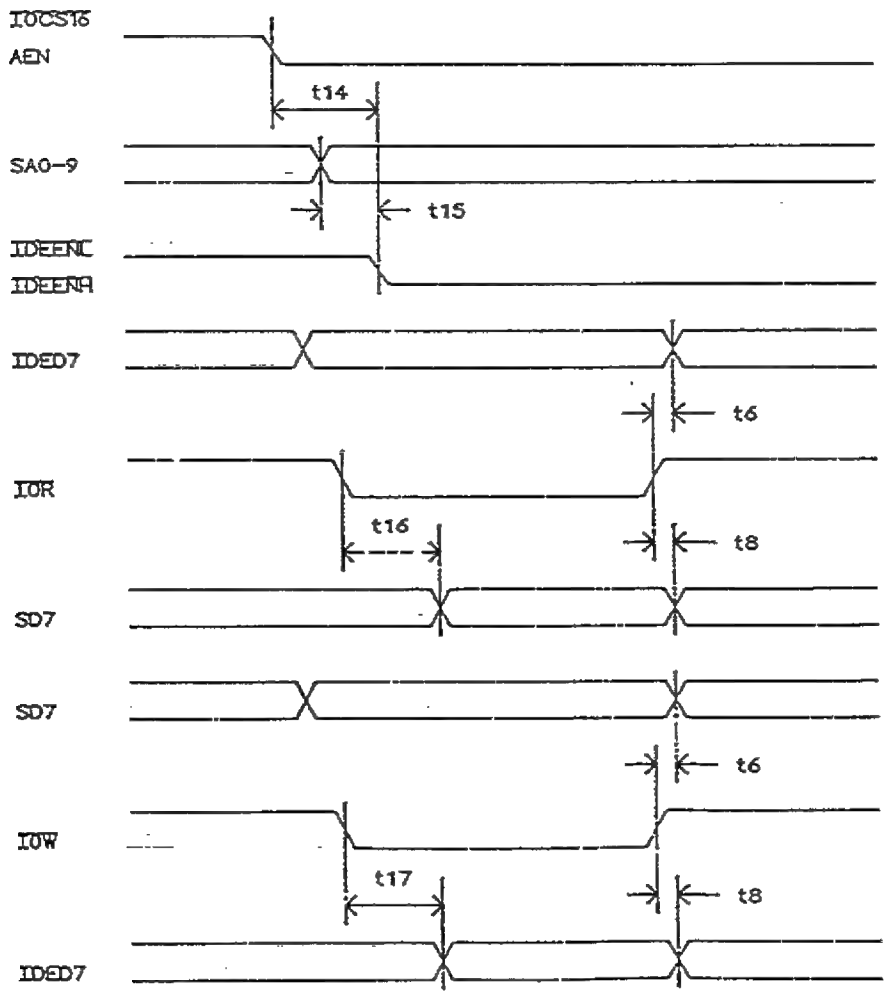
SERIAL PORT TIMING



PARALLEL PORT TIMING



IDE INTERFACE TIMING



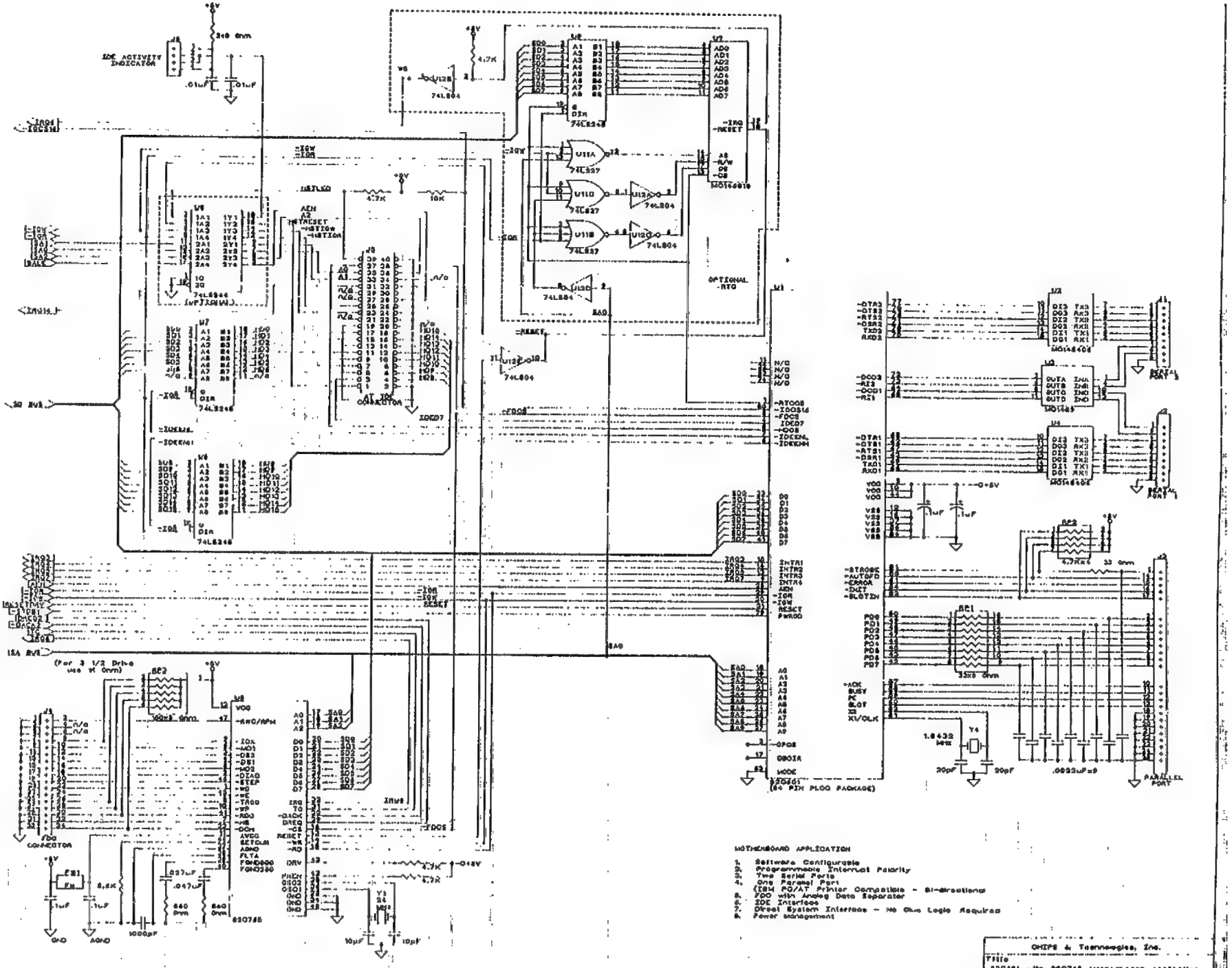

IDE ACTIVITY INDICATOR
MOTHERBOARD APPLICATION
1. Software Configurable
2. Programmable Interrupt Polarity
3. Two Serial Ports
4. One Parallel Port
(IBM PS/AT Printer Compatible - Bi-directional
5. FDD with Analog Data Separator
6. IDE Interface
7. Direct System Interface - No Glue Logic Required
8. Power Management
CHIPS & Technologies, Inc.
Title
82C481 with 82C765 Motherboard Application
Size
Document Number
Rev
Date:
Sheet 22 of 1 at

Figure 8.1

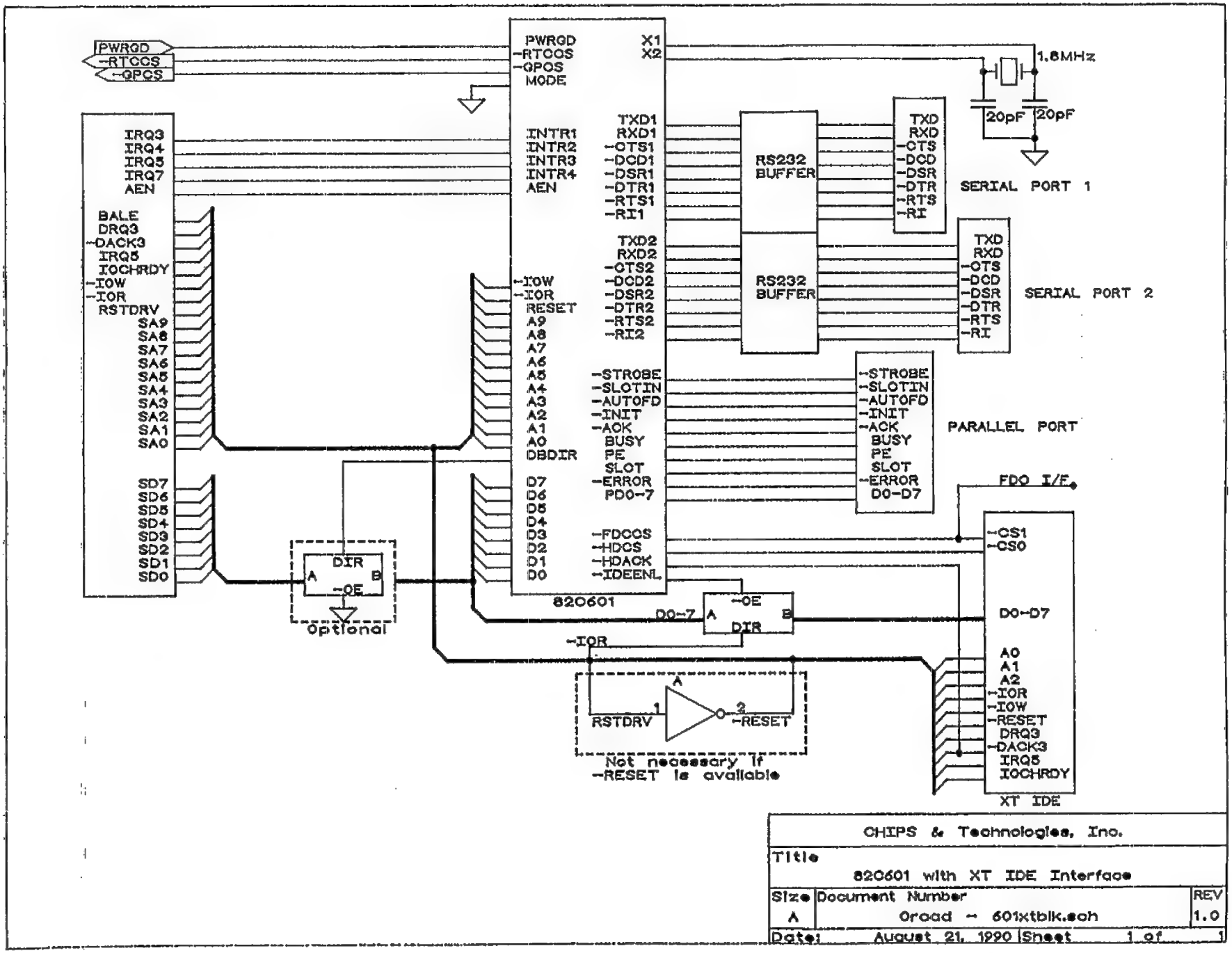

PWRGD
-RTCCS
-QPCS
PWRGD
-RTCCS
-QPCS
MODE
X1
X2
1.8MHz
20pF
20pF
IRQ3
IRQ4
IRQ5
IRQ7
AEN
INTR1
INTR2
INTR3
INTR4
AEN
TXD1
RXD1
-CTS1
-DCD1
-DSR1
-DTR1
-RTS1
-RI1
RS232 BUFFER
TXD
RXD
-CTS
-DCD
-DSR
-DTR
-RTS
-RI
SERIAL PORT 1
BALE
DRQ3
-DACK3
IRQ5
IOCHRDY
-IOW
-IOR
RSTDRV
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
-IOW
-IOR
RESET
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
DBDIR
TXD2
RXD2
-CTS2
-DCD2
-DSR2
-DTR2
-RTS2
-RI2
RS232 BUFFER
TXD
RXD
-CTS
-DCD
-DSR
-DTR
-RTS
-RI
SERIAL PORT 2
-STROBE
-SLOTIN
-AUTOFD
-INIT
-ACK
BUSY
PE
SLOT
-ERROR
PD0-7
-STROBE
-SLOTIN
-AUTOFD
-INIT
-ACK
BUSY
PE
SLOT
-ERROR
D0-D7
PARALLEL PORT
FDD I/F
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
D7
D6
D5
D4
D3
D2
D1
D0
-FDCCS
-HDCS
-HDACK
-IDEENL
DIR
A
B
-OE
optional
820601
D0-7
-OE
A
B
DIR
-IOR
A
1
2
RSTDRV
-RESET
Not necessary if
-RESET is available
-CS1
-CS0
D0-D7
A0
A1
A2
-IOR
-IOW
-RESET
DRQ3
-DACK3
IRQ5
IOCHRDY
XT IDE
CHIPS & Technologies, Inc.
Title
820601 with XT IDE Interface
Size
A
Document Number
Oroad - 601xtblk.sch
REV
1.0
Date:
August 21, 1990
Sheet
1 of
1

Figure 8.2

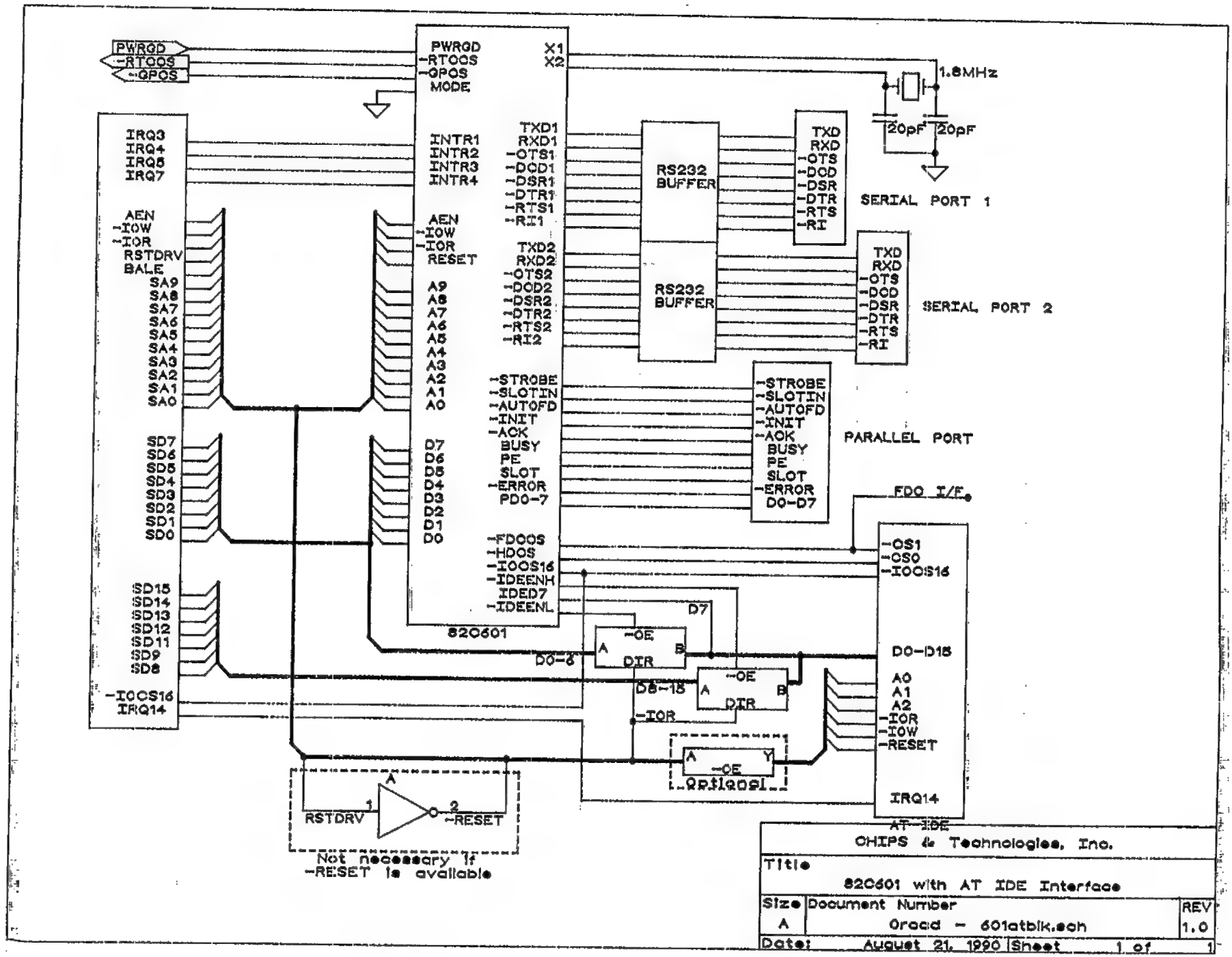

PWRGD
-RTCOS
-GPOS
MODE
X1
X2
1.8MHz
20pF
20pF
IRQ3
IRQ4
IRQ5
IRQ7
INTR1
INTR2
INTR3
INTR4
TXD1
RXD1
-OTS1
-DCD1
-DSR1
-DTR1
-RTS1
-RI1
RS232 BUFFER
TXD
RXD
-OTS
-DCD
-DSR
-DTR
-RTS
-RI
SERIAL PORT 1
AEN
-IOW
-IOR
RSTDRV
BALE
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
RESET
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
TXD2
RXD2
-OTS2
-DCD2
-DSR2
-DTR2
-RTS2
-RI2
RS232 BUFFER
SERIAL PORT 2
-STROBE
-SLOTIN
-AUTOFD
-INIT
-ACK
BUSY
PE
SLOT
-ERROR
PD0-7
PARALLEL PORT
D0-D7
FDD I/F
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
D7
D6
D5
D4
D3
D2
D1
D0
-FDCOS
-HDCS
-IOCS16
-IDEENH
IDED7
-IDEENL
820601
-OS1
-OS0
-IOCS16
D7
-OE
A
B
DIR
D0-D15
D0-8
D8-15
A0
A1
A2
-IOR
-IOW
-RESET
IRQ14
SD15
SD14
SD13
SD12
SD11
SD9
SD8
-IOCS16
IRQ14
A
Y
-OE
Optional
A
1
2
RSTDRV
-RESET
Not necessary if
-RESET is available
AT-IDE
CHIPS & Technologies, Inc.
Title
820601 with AT IDE Interface
Size
A
Document Number
Orcad - 601atblk.sch
REV
1.0
Date:
August 21, 1990
Sheet
1 of
1

Figure 8.3

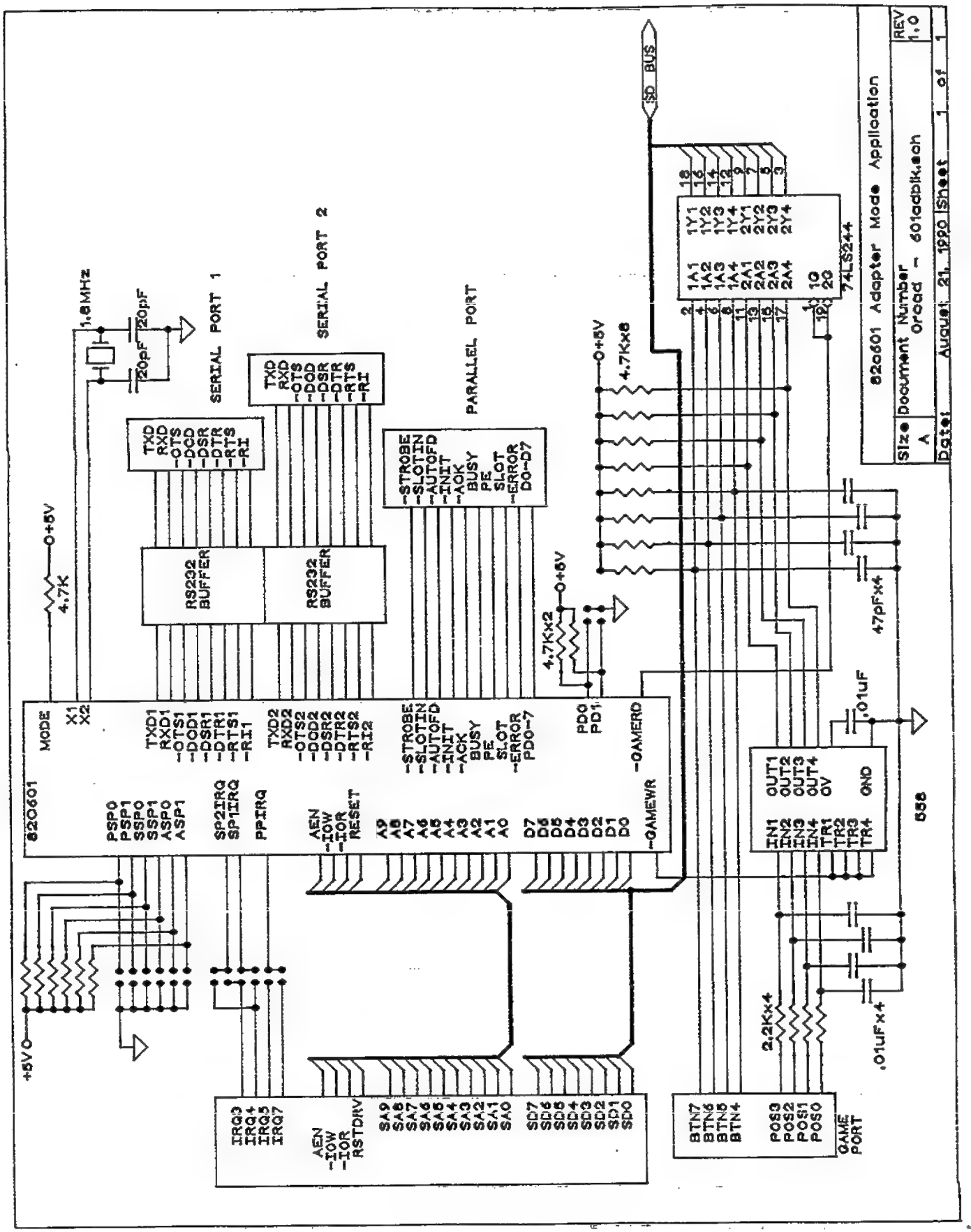
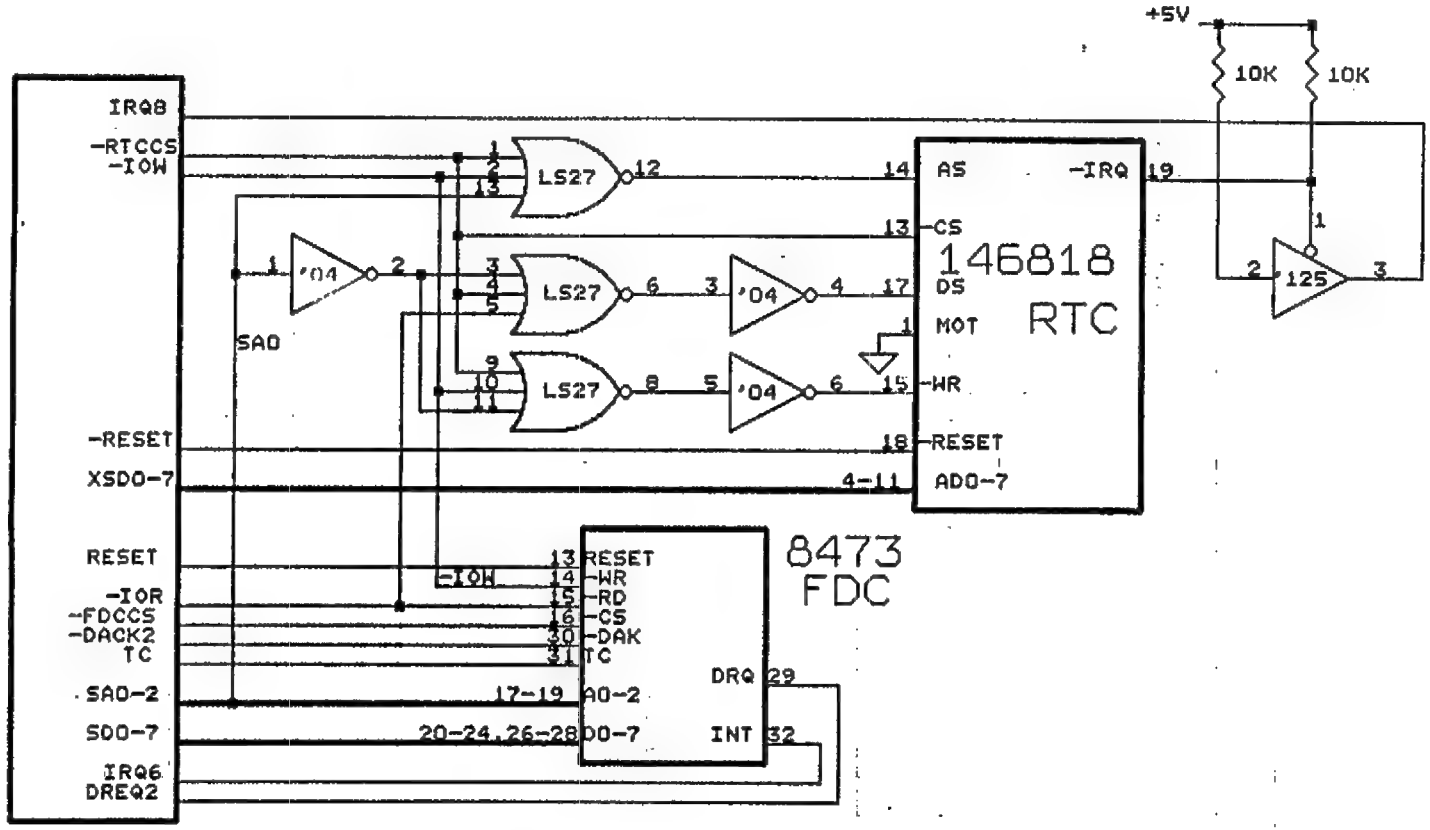
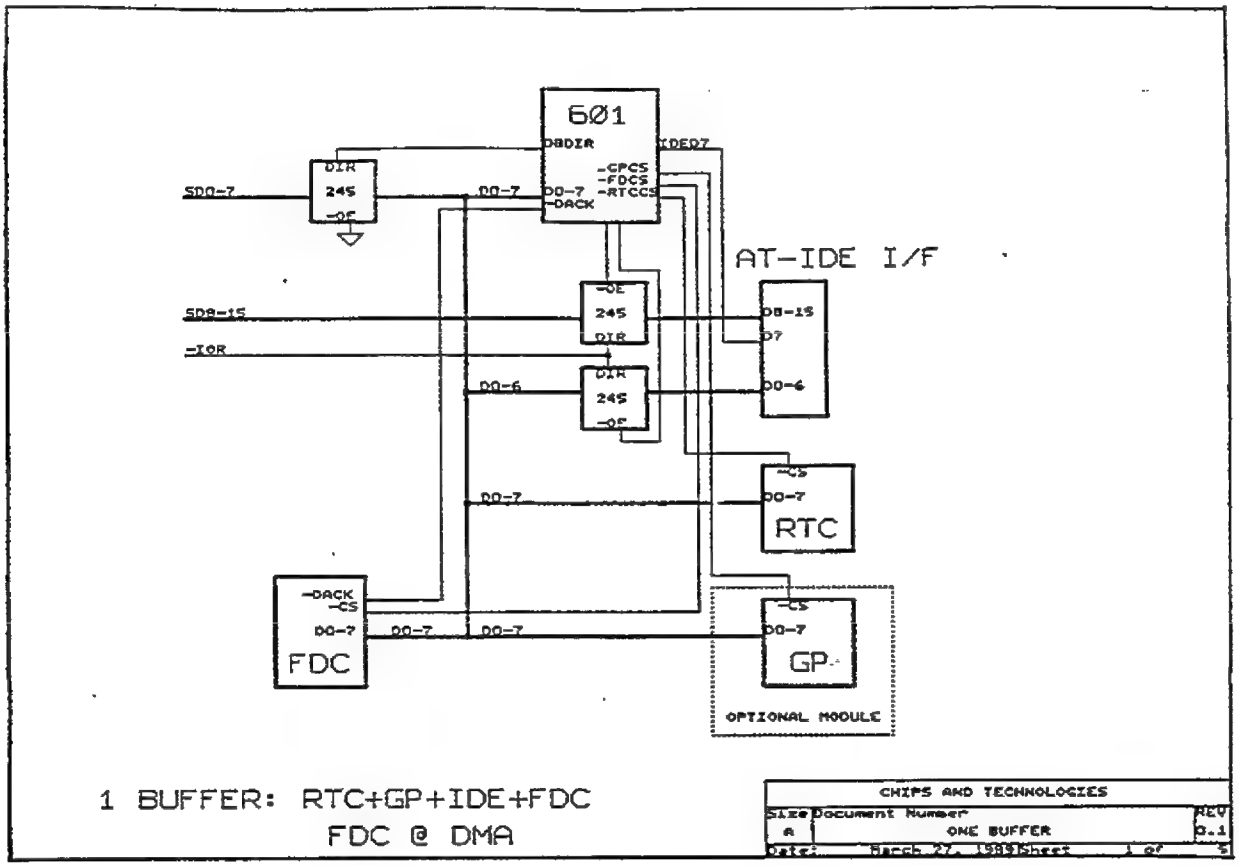

SD BUS
SERIAL PORT 1
SERIAL PORT 2
PARALLEL PORT
RS232 BUFFER
RS232 BUFFER
74LS244
820601
MODE
GAME PORT
820601 Adapter Mode Application
Size: A
Document Number: 0road - 601adptk.sch
REV: 1.0
Date: August 21, 1990
Sheet 1 of 1

Figure 8.4



CHIPS AND TECHNOLOGIES		
Size	Document Number	REV
A	82C601 FDC & RTC INTERFACE	0.3
Date: June 16, 1989	Sheet 3 of 4	


601
DBDIR
IDED7
-CPCS
-FDCS
-RTCCS
DO-7
-DACK
SDO-7
DIR
245
-OE
SD8-15
-IOR
AT-IDE I/F
D8-15
D7
D0-6
-CS
RTC
-DACK
FDC
GP
OPTIONAL MODULE
1 BUFFER: RTC+GP+IDE+FDC
FDC @ DMA
CHIPS AND TECHNOLOGIES
Size
Document Number
ONE BUFFER
REV
0.1
Date:
March 27, 1989
Sheet
1 of
5

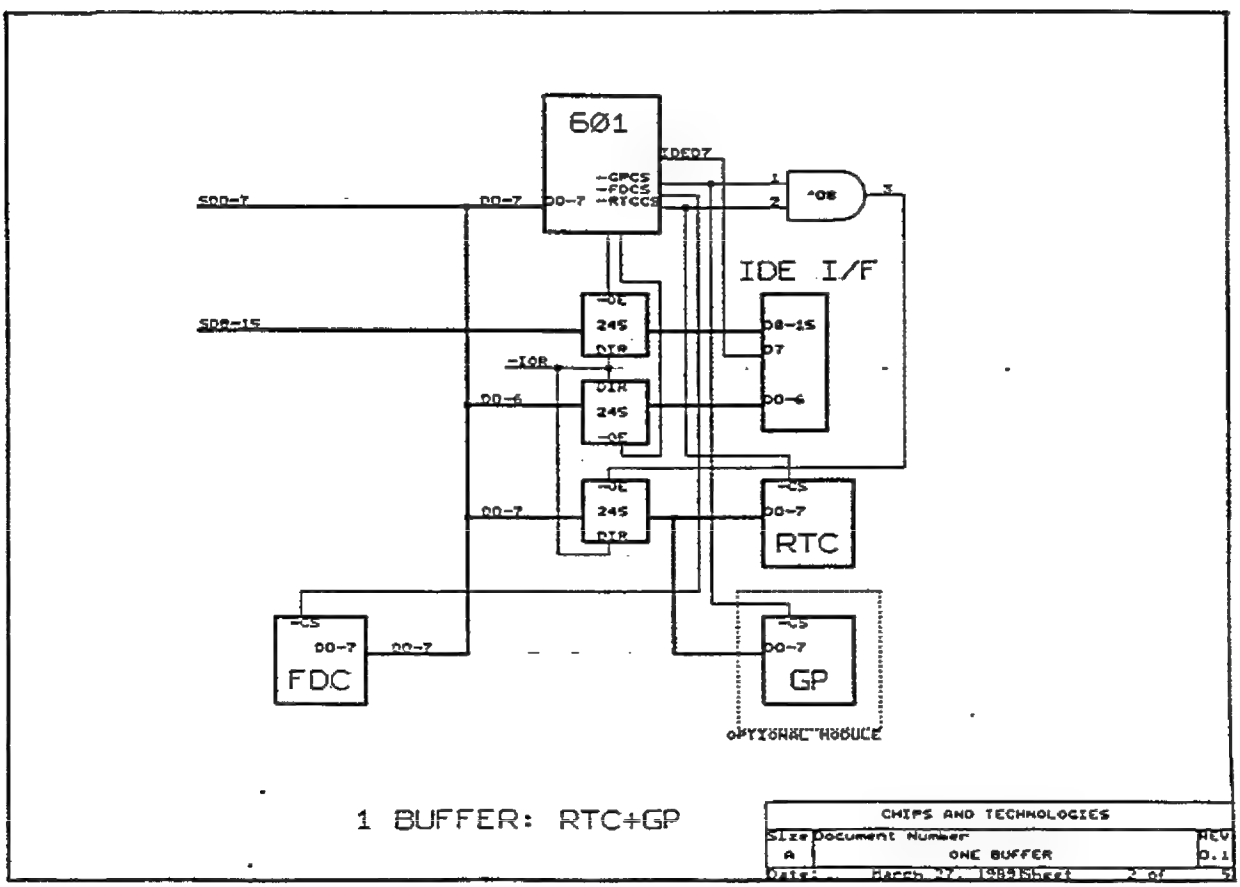

601
IDED7
-CPCS
-FDCS
-RTCCS
SDO-7
DO-7
SD8-15
-IOR
IDE I/F
D8-15
D7
D0-6
-CS
RTC
FDC
GP
1 BUFFER: RTC+GP
CHIPS AND TECHNOLOGIES
Size
Document Number
ONE BUFFER
REV
0.1
Date:
March 27, 1989
Sheet
2 of
5

Figure 8.6

F82C601 (PFP) PINOUT - 80 PINS

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	Vss	21	D0	44	-ACK	66	-IOCS16
2	INTR3	22	D1	45	BUSY	66	(SSP1)
2	(PPIRQ)	23	D2	46	PE	67	X1
3	INTR2	24	D3	47	SLCT	68	X2
3	(SP1IRQ)	25	Vss	48	-ERROR	69	MODE
4	INTR1	26	D4	49	-CTS1	70	Vss
4	(SP2IRQ)	27	D5	50	-DSR1	71	(PP1)
5	Vss	28	D6	51	-DCD1	71	-RTCCS
6	DBDIR	29	D7	52	-RI1	72	Vcc
7	A0	30	PD7	53	RXD1	73	-GPCS
8	A1	31	PD6	54	-RTS1	73	(PP0)
9	A2	32	Vcc	55	-DTR1	74	IDED7
10	A3	33	PD5	56	TXD1	74	(PSP1)
11	A4	34	PD4	57	-CTS2	75	-HDCS
12	A5	35	PD3	58	-DSR2	75	(PSP0)
13	A6	36	PD2	59	-DCD2	76	(-GAMEWR)
14	A7	37	PD1	60	-RI2	76	-IDEENH
15	A8	38	PD0	61	RXD2	77	(-GAMERD)
16	A9	39	-STROBE	62	-RTS2	77	-IDEENL
17	AEN	40	-SLCTIN	63	-DTR2	78	(ASP0)
18	-IOR	41	-INIT	64	TXD2	78	-FDCS
19	-IOW	42	-AUTOFD	65	PWRGD	79	(ASP1)
20	RESET	43	Vss	65	(SSP0)	79	INTR4
						80	Vcc

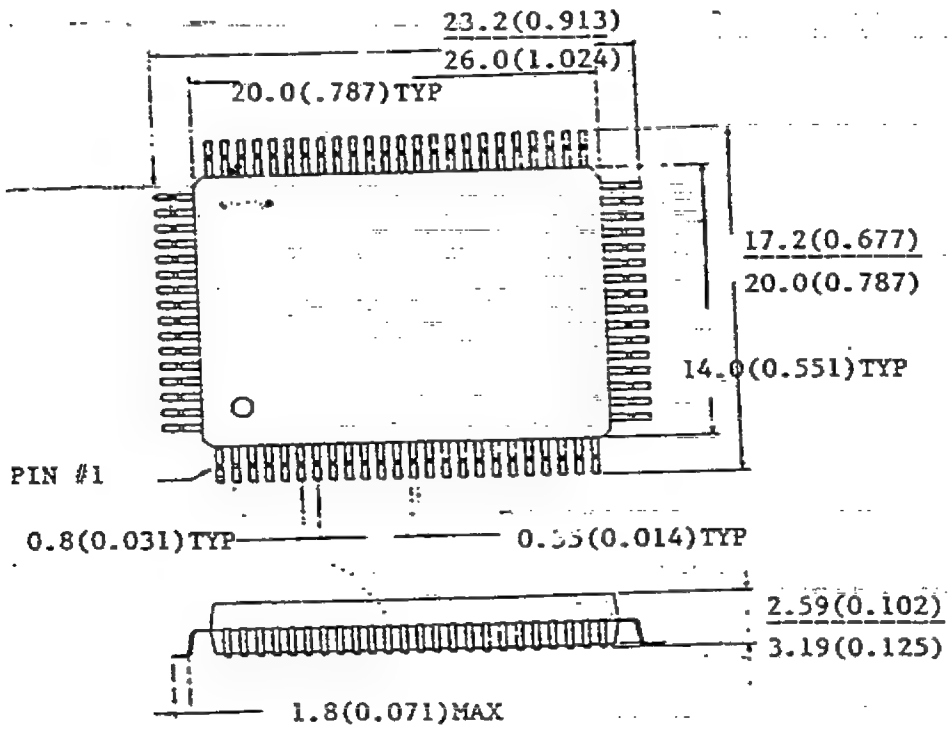
F82C610 (PFP) PINOUT - 80 PINS

NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN
A0	7	D5	27	INTR4	79	-RTCCS	71
A1	8	D6	28	-IOCS16	66	-RTS1	54
A2	9	D7	29	-IOR	18	-RTS2	62
A3	10	DBDIR	6	-IOW	19	RXD1	53
A4	11	-DCD1	51	MODE	69	RXD2	61
A5	12	-DCD2	59	PD0	38	SLCT	47
A6	13	-DSR1	50	PD1	37	-SLCTIN	40
A7	14	-DSR2	58	PD2	36	(SP1IRQ)	3
A8	15	-DTR1	55	PD3	35	(SP2IRQ)	4
A9	16	-DTR2	63	PD4	34	(SSP0)	65
-ACK	44	-ERROR	48	PD5	33	(SSP1)	66
AEN	17	-FDCS	78	PD6	31	-STROBE	39
(ASP0)	78	(-GAMERD)	77	PD7	30	TXD1	56
(ASP1)	79	(-GAMEWR)	76	PE	46	TXD2	64
-AUTOFD	42	-GPCS	73	(PP0)	73	Vcc	32
BUSY	45	-HDCS	75	(PP1)	71	Vcc	72
-CTS1	49	IDED7	74	(PPIRQ)	2	Vcc	80
-CTS2	57	-IDEENH	76	(PSP0)	75	Vss	1
D0	21	-IDEENL	77	(PSP1)	74	Vss	5
D1	22	-INIT	41	PWRGD	65	Vss	25
D2	23	INTR1	4	RESET	20	Vss	43
D3	24	INTR2	3	-RI1	52	Vss	70
D4	26	INTR3	2	-RI2	60	X1	67
						X2	68

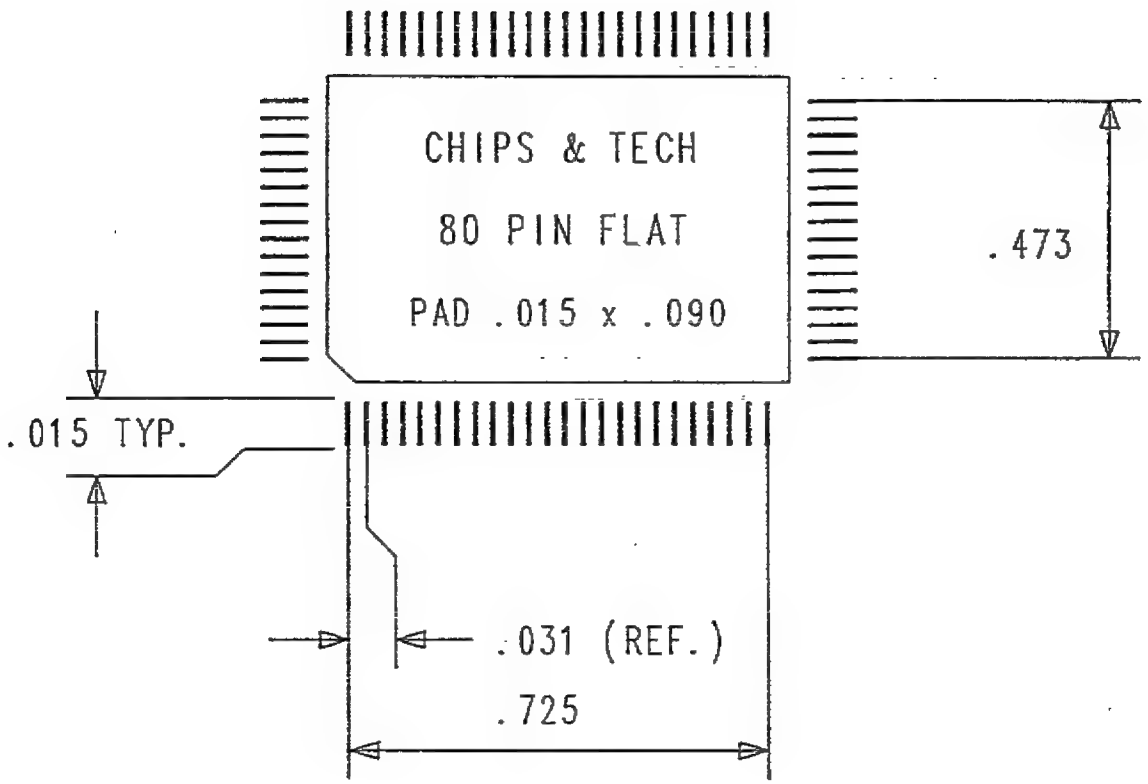
Chips and Technologies, Incorporated

80 PIN PLASTIC FLAT PACKAGE (RECTANGULAR)

DIMENSIONS: mm (in)



DRAWING NO.: 80RPFP-01



SCALE 3x

P82C601 (PLCC) PINOUT - 84 PINS

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	(PP1)	15	INTR1	38	D4	62	-CTS1
1	-RTCCS	15	(SP2IRQ)	39	D5	63	-DSR1
2	Vcc	16	Vss	40	D6	64	-DCD1
3	-GPCS	17	DBDIR	41	D7	65	-RI1
3	(PP0)	18	A0	42	PD7	66	RXD1
4	IDED7	19	A1	43	PD6	67	-RTS1
4	(PSP1)	20	A2	44	Vcc	68	-DTR1
5	-HDCS	21	A3	45	PD5	69	TXD1
5	(PSP0)	22	A4	46	PD4	70	-CTS2
6	(-GAMEWR)	23	A5	47	PD3	71	-DSR2
6	-IDEENH	24	A6	48	PD2	72	-DCD2
7	(-GAMERD)	25	A7	49	PD1	73	-RI2
7	-IDEENL	26	A8	50	PD0	74	N/C
8	(ASP0)	27	A9	51	-STROBE	75	RXD2
8	-FDCS	28	AEN	52	-SLCTIN	76	-RTS2
9	(ASP1)	29	-IOR	53	N/C	77	-DTR2
9	INTR4	30	-IOW	54	-INIT	78	TXD2
10	Vcc	31	RESET	55	-AUTOFD	79	PWRG
11	N/C	32	N/C	56	Vss	79	(SSP0)
12	Vss	33	D0	57	-ACK	80	-IOCS16
13	INTR3	34	D1	58	BUSY	80	(SSP1)
13	(PPIRQ)	35	D2	59	PE	81	X1
14	INTR2	36	D3	60	SLCT	82	X2
14	(SP1IRQ)	37	Vss	61	-ERROR	83	MODE
						84	Vss

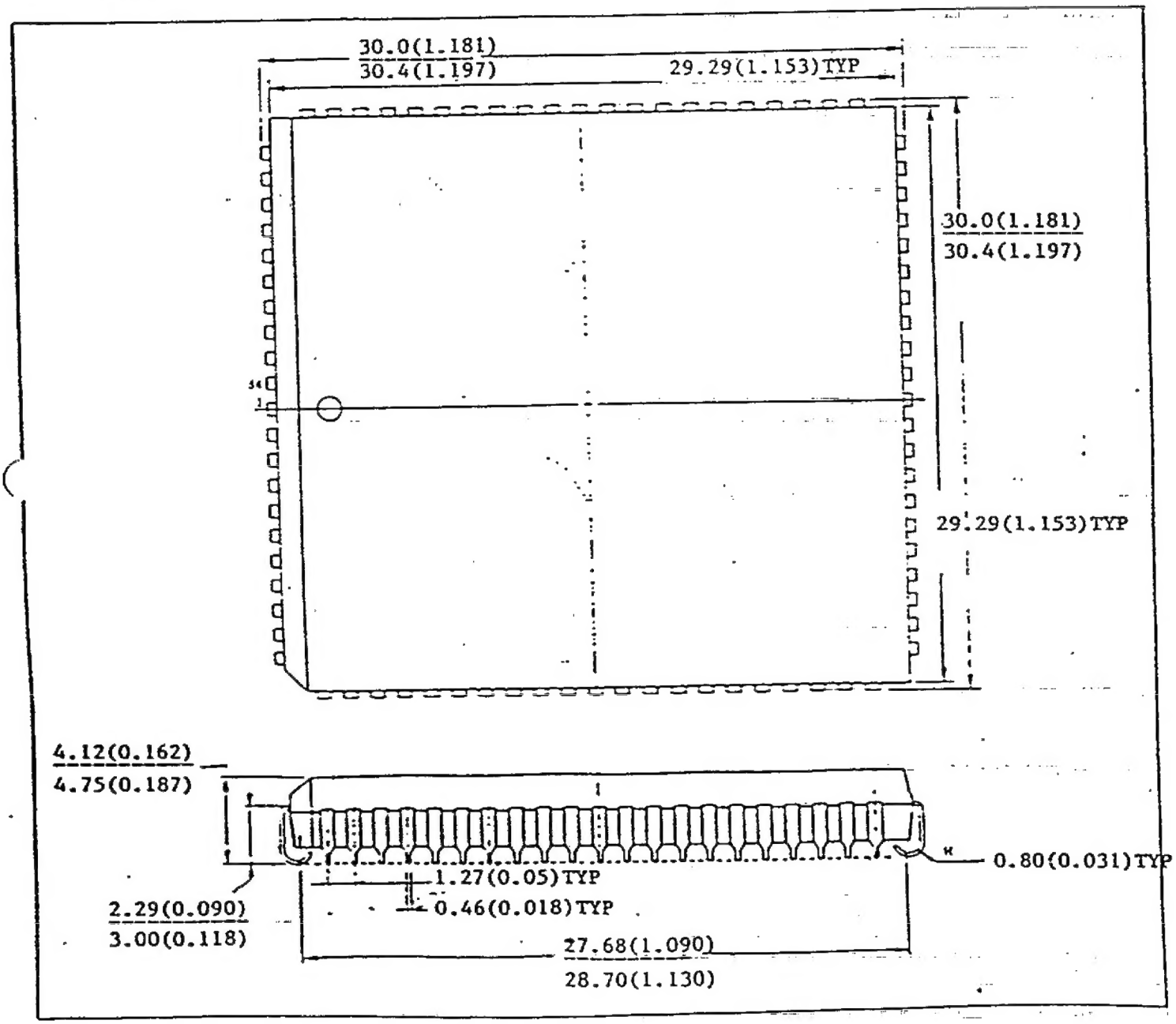
P82C601 (PLCC) PINOUT - 84 PINS

NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN
A0	18	D6	40	-IOR	29	-RI2	73
A1	19	D7	41	-IOW	30	-RTCCS	1
A2	20	DBDIR	17	MODE	83	-RTS1	67
A3	21	-DCD1	64	N/C	11	-RTS2	76
A4	22	-DCD2	72	N/C	32	RXD1	66
A5	23	-DSR1	63	N/C	53	RXD2	75
A6	24	-DSR2	71	N/C	74	SLCT	60
A7	25	-DTR1	68	PD0	50	-SLCTIN	52
A8	26	-DTR2	77	PD1	49	(SP1IRQ)	14
A9	27	-ERROR	61	PD2	48	(SP2IRQ)	15
-ACK	57	-FDCS	8	PD3	47	(SSP0)	79
AEN	28	(-GAMERD)	7	PD4	46	(SSP1)	80
(ASP0)	8	(-GAMEWR)	6	PD5	45	-STROBE	51
(ASP1)	9	-GPCS	3	PD6	43	TXD1	69
-AUTOFD	55	-HDCS	5	PD7	42	TXD2	78
BUSY	58	IDED7	4	PE	59	Vcc	2
-CTS1	62	-IDEENH	6	(PP0)	3	Vcc	10
-CTS2	70	-IDEENL	7	(PP1)	1	Vcc	44
D0	33	-INIT	54	(PPIRQ)	13	Vss	12
D1	34	INTR1	15	(PSP0)	5	Vss	16
D2	35	INTR2	14	(PSP1)	4	Vss	37
D3	36	INTR3	13	PWRGD	79	Vss	56
D4	38	INTR4	9	RESET	31	Vss	84
D5	39	-IOCS16	80	-RI1	65	X1	81
						X2	82

Chips and Technologies, Incorporated

84-Pin PLCC

DIMENSIONS: mm (in)



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